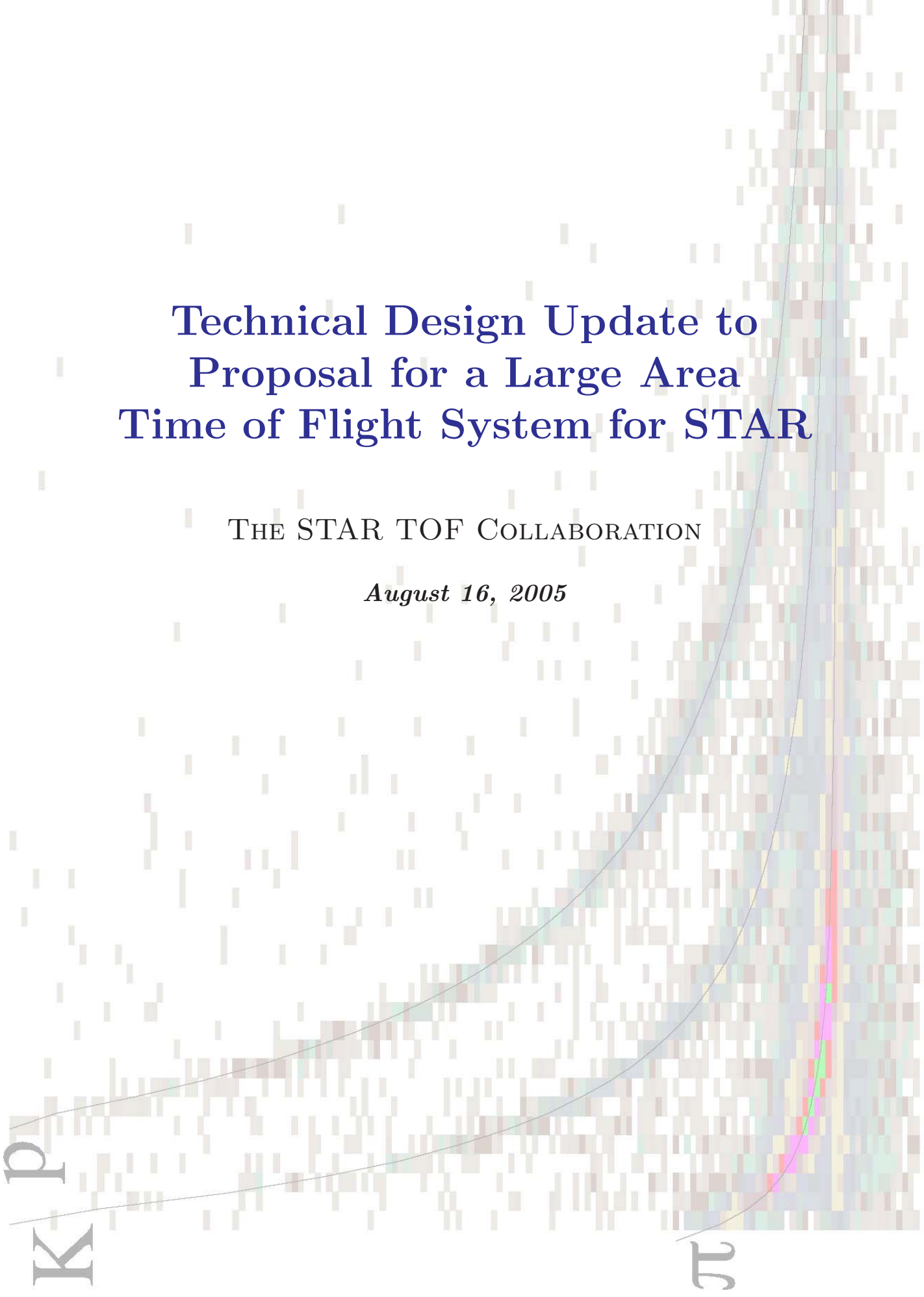
Technical Design Update to Proposal for a Large Area Time of Flight System for STAR

The STAR TOF Collaboration

August 16, 2005



Technical Design Update

STAR-TOF

(The STAR TOF Collaboration)

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1 Introduction

The STAR Collaboration has proposed building a 23,040-channel multi-gap resistive plate chamber (MRPC) time-of-flight (TOF) system to be installed at the outer radius of the time projection chamber (TPC). This area is now occupied by the central trigger barrel (CTB), see figure 1. The detector will cover the full 2π in azimuth and from -0.9<η<0.9 in pseudo-rapidity. The MRPC is a major new detector technology developed originally for the ALICE experiment at CERN. Also part of the present project is the construction of a large-area start detector appropriate for the large-area MRPC stop detector. The document "Proposal for a Large-Area Time-of-Flight System for STAR, May 24, 2004" may be found at Ref. [1].

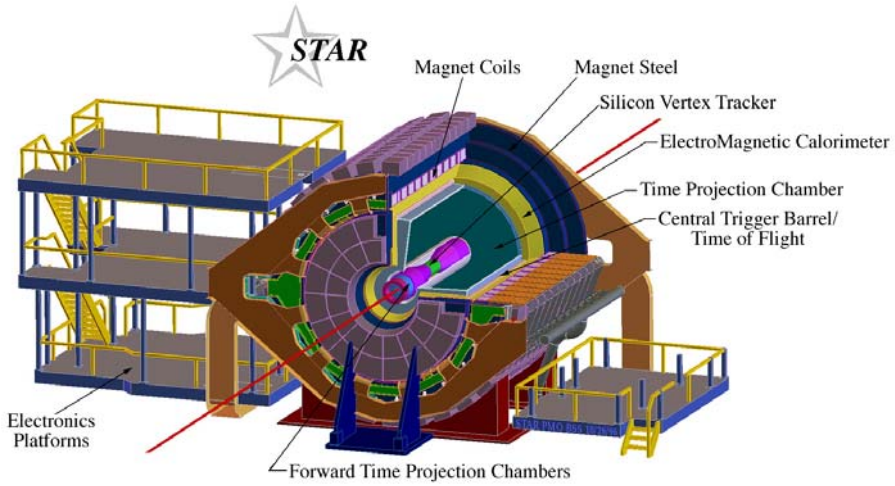


Figure 1: A cut-away view of the STAR detector showing the major subsystems. The TOF system is indicated just outside the TPC and just inside the barrel EMC.

STAR has been conducting successful R&D for STAR-specific MRPC detectors since 2000. Prototype detectors have been successfully operated in STAR in Runs 3, 4, and 5 (2002-2005). A description of the prototype detectors as well as the results from the STAR operations can be found in the proposal and in this technical update. While providing a wealth of information on the successful operation of MRPCs in a real experiment, the prototype systems also resulted in interesting physics results on identified hadron transverse momentum distributions [2], and open charm production [3]. The following is a brief summary of the information provided by this technical update.

Tray mechanical design – The proposed mechanical design for the TOF tray for the full system will have only minor changes from the prototype TOF tray, "TOFr5," installed for Run-5. This design allows, for the first time, the connection of the modules to the high voltage (HV) distribution wire, and the connection of the signal cables to the electronics while the tray is still "open." This will allow for testing of

the HV distribution, as well as signal connectivity while the tray is open, which will greatly facilitate finding and fixing any problems. A plan for building and testing trays is presented.

TOFr5 Power, Temperature, and Heat-Flow Tests – The TOFr5 tray has an integral copper cooling loop which was connected to the STAR modified-chilled-water distribution system. Tests in the laboratory indicate that the cooling loop removes 105W of the 140W of heat generated on the tray. We plan to test a solid cover for the tray electronics and estimate that this will increase the efficiency of the cooling loop to ∼95%. In addition, we expect that the use of the ALICE/Bologna "NINO" front-end chip will reduce the power consumption of the tray to ∼100W.

Electronics – Almost all of the functionality of the final electronics system required for the large-area TOF was provided by the Run-5 prototype electronics. This included the on-board digitization and readout of start and stop times relative to a master clock using the CERN HPTDC, and the installation of the CERN/Alice DDL fiber interface to transmit data to STAR DAQ. The remaining functions to be implemented in the full system are the 9.4 MHz multiplicity information provided to the Level-0 trigger, and the "THUB" data collection and interface card. In addition, we are designing and plan to test a new front-end board using the ALICE/Bologna "NINO" chip. The motivation for this latter development is to reduce cost, to reduce power consumption, and perhaps to improve the timing performance.

Low Voltage Power Supply System – Tests of Wiener switching power supplies in Run-5 indicate that they will perform successfully in the TOF system. This change results in a great reduction in rack space compared to linear supplies and a corresponding reduction in infrastructure costs.

Start Detector – The conceptual design for a mesh-dynode PMT start detector presented in the proposal is further developed. Simulations of the efficiency in low-multiplicity collisions for a number of configurations are presented. The development of a high-rate low-power PMT base is also described.

Preliminary Analysis of the Run 5 Data – Preliminary analysis of the Run 5 TOF data indicates a ∼105ps timing resolution in the 200 GeV Cu+Cu data and ∼135ps in the 62 GeV data. The contribution of the start-side timing to those results are ∼50 ps and ∼85 ps, respectively. An upgraded start detector with many more read-out channels would significantly improve the start-side timing performance and overall efficiency.

2 Tray mechanical design

2.1 Introduction

The tray mechanical design has benefitted from the fact that three generations of MRPC-based trays that have been built "from the ground up" and operated in STAR during entire RHIC runs. The first generation prototype, "TOFr" was installed during Run-3, "TOFr-prime" was installed during Run-4, and "TOFr5" was installed during Run-5. The evolution of the tray design over these generations, and the next, "TOFr6," has improved the tolerances, especially on the MRPC positioning. It has also made the fabrication simpler and more repeatable, hence reducing the labor required.

The fabrication procedure is tightly tied to a specific mechanical design. The overall design of the tray can be broken into the following general areas.

- **MRPC placement** - Each of 32 MRPC detectors must be held in place at a specific position and angle with respect to the tray. Each MRPC is held in place (to $\pm$50 mils) in the STAR-ϕ direction by the long vertical walls of the tray's bottom assembly (5 of the six walls of the gas box). The positioning of interest thus boils down to the module (Y,Z) values and angles, $\theta_{\rm yz}$, with respect to the tray's long axis. The very limited space available for the MRPC placement and other constraints make the placement strategy a somewhat subtle subject. It is not possible to place every MRPC module so as to be normal to Z=0. It also does not seem to be necessary, based on the test-beam and STAR experience. One ends up placing MRPCs in groups of the same angle, while trying to limit the variation in the angles with respect to the normal to Z=0 to $\pm$10 degrees or so. Numerous reasonable placement schemes exist. For whatever scheme is chosen, the smearing of the primary vertex results in η-gaps in the TOF coverage for the trays on the same side (in Z) as the primary vertex, and increases the probability for multiple MRPC hits per track for the trays on the other side (a pro and a con, but certainly a complication).

- **MRPC to FEE connection** - Each of the six pad-pairs from each of the 32 MRPC modules (192 channels total) must be connected to the front-end electronics.

- **Gas box sealing** - The MRPCs must be bathed in a flowing gas, and the volume that contains this gas must not leak. The sealant must be resistant to constant exposure to freon and isobutane.

- **Interface to the Electronics** - The front-end electronics require careful mechanical mounting so as to avoid all stresses to the boards. The sixth wall of the gas box is mostly a layer of electronics boards sealed to the tray body.

- **Cooling** - An efficient *local* removal of the heat generated by the on-board electronics is needed to make the smallest possible impact on the neighboring

STAR detectors (TPC inside and EMC outside). This also improves the performance of the MRPC detectors, as warm MRPCs draw more current and exhibit elevated noise and streamer rates.

- **Electronics protection/cable strain relief** - Mechanical protection of the electronics is needed since the tray test and installation procedures require that the trays be picked up and moved around by hand in arbitrary ways without damaging anything. The cabling leaving the on-board electronics must fit within this outer protective cover and be strain-relieved to insure consistent data and control connections.

- **STAR integration** - The overall size of the tray and specific mechanical tolerances must meet requirements, agreed to by the STAR Technical Support Group (STSG), to insure that the trays are easy and safe to install in STAR. The cabling, facilities requirements, installation plan, and safety reviews also require coordination with STSG and STAR Operations.

The ultimate goal of this design effort is a mechanical design, and a matching fabrication plan, for final TOF trays that:

- fit into the very small space available inside STAR, including the two layers of on-board electronics, its cabling, and an outer protective cover.

- have the MRPCs placed as normal to Z=0 as possible, and with the minimum number of 'additional' η gaps.

- are assembled as much as possible using parts fabricated by machine (out-of-house or on UT's Hurco machines), to take advantage of the typically tighter fabrication and assembly tolerances and also the decreased manpower requirements.

- uses pre-tested electronics and pre-qualified MRPC modules to reduce as much as possible the number of trays that need to be reopened after final assembly to fix some internal problem. The tray mechanical pieces also need to be pre-qualified to insure the whole assembly will fit together correctly at the end.

- allows specific connectivity tests at intermediate stages of the final assembly.

- makes the final assembly as safe and repeatable as possible.

- conforms to STSG-agreed specifications for the tray installation, insuring that this and the commissioning stages are safe and straight-forward.

- are ultimately leak-less and as light as possible, to limit the impact of the TOF system on the neighboring STAR subsystems.

The following sections 2.1.1, 2.1.2, and 2.1.3 describe the evolution of the mechanical design over the last three RHIC runs. Section 2.1.4 gives a general description of the expected design of the next tray"TOFr6." A summary of the mechanical design aspects of these four generations is presented in section 2.2. A discussion of the final trays for the large-area system is presented in sections 2.3 and 2.4.

2.1.1 Run-3 TOFr mechanical design

The TOFr tray of RHIC Run-3 was our first attempt at an installation of the MRPC technology in STAR. The basic idea was to get the MRPCs in a modified CTB tray, and to develop front-end electronics to drive long cables for digitization in CAMAC by the existing STAR TOFp system.

The "bottom assembly" used for TOFr was simply a refurbished CTB final-prototype tray. This is 50mil-thick aluminum stamped, braked, and edge-welded into five of the six walls of the MRPC gas volume. The "feet," which hold the tray in place with respect to the STAR TPC, were attached to the underside of this box with ∼20 punch rivets. These rivets, and the interior edges of the bottom assembly were covered with several layers of (an arbitrary) sealant.

The MRPCs were held in place with respect to the interior of the bottom assembly by so-called "sawtooths." These were specifically-shaped pieces of 1/4"-thick NOMEX[1]. The CADD layout of these pieces was printed at 1:1 scale[2] onto paper that was pasted with double-sided tape onto two layers of NOMEX also joined by double-sided tape. The shapes were then cut out by hand using a bandsaw, requiring something like a technician-day for the one TOFr tray. Once cut, the two pieces of NOMEX were separated from each other and then glued as mirror images to the two inner surfaces of the long vertical walls of the tray bottom assembly. Approximately 50 different shapes were necessary to place the twenty-eight (28) MRPCs in TOFr. The NOMEX is extremely rigid and hence well-matched to the mounting strategy for this tray, but fiberglass is not particularly popular to machine and the edges of the pieces can be *sharp*. Each piece must be positioned by hand individually as it is glued into place surrounding one or more MRPCs. Given typical adhesive curing times and a finite of number of clamps, the MRPC installation into the TOFr bottom assembly took ∼2 technician-days.

Figure 2 shows the $\eta\sim0$ end of the TOFr bottom assembly filled with the MRPCs held in place by the sawtooth pieces.

The sixth wall of the gas box is the combination of the "rail assembly" and a layer of electronics boards that are bolted and sealed to this rail assembly. This composite assembly is then bolted and sealed to the filled bottom assembly (*cf.* figure 2).

The rail assembly was made by welding together of four different 1/2"×1/2"×1/8" aluminum angle pieces and 1/8"-thick aluminum "cross-piece" plates. Approximately

[1] Phenolic-impregnated Kraft-paper honeycomb with fiberglass backing sheets on both sides.

[2] It was necessary to account for a 0.5% scaling of the printed versions along the long axis of the printed pages!

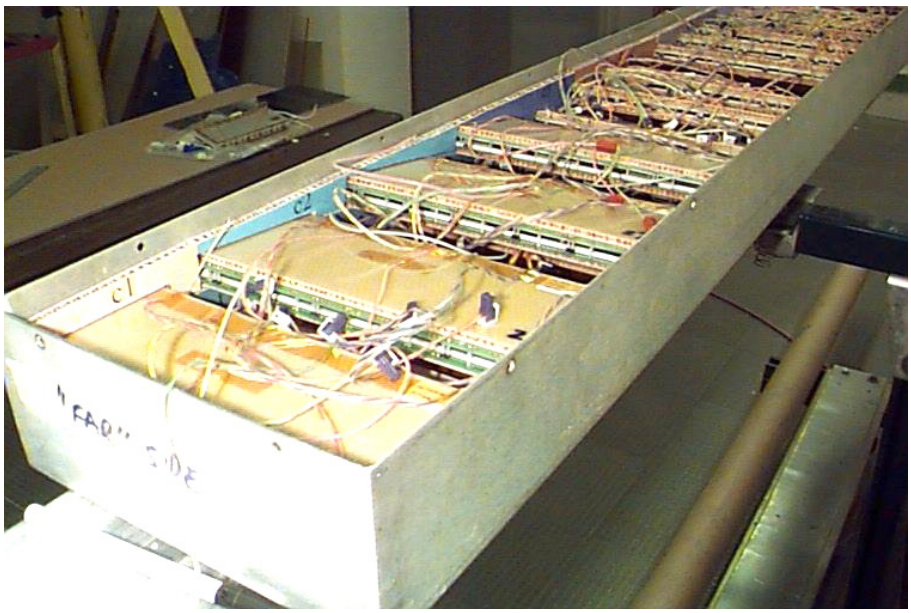


Figure 2: The interior of the TOFr tray near the $\eta\sim0$ end. Seen are the MRPCs, six twisted-pair signal pigtails per MRPC, and the sawtooths pieces inside a standard CTB bottom assembly.

200 through-holes were tapped into the rail assembly to mechanically tie the electronics and the bottom assembly to the rail assembly. The fabrication of this rail assembly required a technician-week. It is shown in Figure 3 test-mounted into the (empty) bottom assembly.

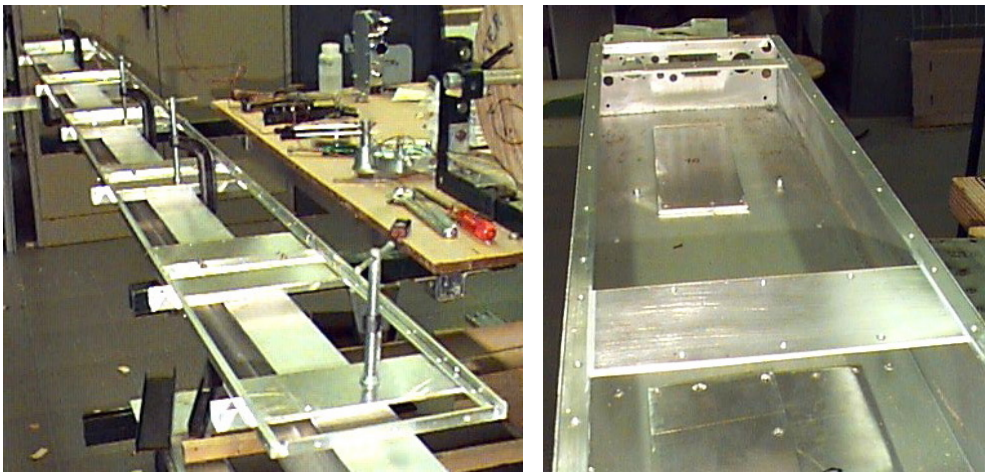


Figure 3: On the left, the TOFr rail assembly during the welding together of the tapped aluminum angle pieces and the cross-pieces. On the right, the completed rail assembly temporarily installed onto the bottom assembly.

The 28 MRPCs consisted of 24 modules produced at USTC and 4 "CERN" mod-

ules. The nineteen USTC MRPCs with the best noise rates (on the bench) were placed on one HV bus (bus "A"), and the 4 cern modules and the noisiest 5 USTC modules were placed on a separate bus "B".

The on-board electronics for this run consisted of a layer of "feed-through" (F/T) boards that close the gas box and also have only a few components (preamplification and input protection only). A second layer of electronics, the 'TOFr FEE' boards', amplified and discriminated the signals and sent these along long cables for digitization in CAMAC. Most of the power dropped by the on-board electronics was dropped on the FEE boards, which were separated from the closest wall of the MRPC gas box by an air gap.

A gasket approach was used to seal the F/T boards to the rail assembly. One side of the gaskets (1mm-thick neoprene) were glued in place onto the rail assembly and the opposite side of the gaskets were greased. This approach was labor-intensive (few technician-days) and ugly to fabricate as the gasket glue is maddeningly sticky and stringy. This was our very first attempt at a full tray of MRPCs and we wanted to allow for the possibility that we might need to break into the gas volume often to fix problems.[3]

Upon final assembly, a few leaks were found from the gasket to FEE interface. Re-torquing helped, but ultimately there was enough concern about the long-term stability of this gas seal that additional sealant was placed around all outer edges of these gaskets. In most places this was overkill, and ugly to look at, but it worked, as the result was sufficiently leak-less according to sensitive tests. The sealant chosen was arbitrary and proved to be suspect. An obvious discoloration of the sealant was observed at the end of Run-3.

Figure 4 shows the final-assembled TOFr tray under gas and HV while under noise testing at Rice. The $\eta\sim0$ end is in the foreground. Most of the signal pigtail cables are not connected in this picture, although one can see 12 of them connected to one FEE board (one MRPC module, six detector channels) at the end of the F/T board closest to the camera. The overall height of tray, especially when including the height of all $\sim$400 signal pigtails, violated the integration volume by several inches, but there wasn't a BEMC module installed in the location behind TOFr during Run-3.

There was no local cooling for this tray. However, there was an air gap between the FEE layer (which dropped the majority of the power) and the F/T layer which closed the MRPC gas box. The on-board electronics did not significantly heat the MRPC volume and the detectors showed noise rates that were low enough to make a cooling scheme unnecessary.

2.1.2 Run-4 TOFr-prime mechanical design

The so-called "TOFr-prime" tray was the second-generation full-sized prototype built specifically for, and operated throughout, Run-4. The MRPCs used were a combi-

[3] In the end we decided to break into the tray only once, and only in order to look into a few bad channels during the d+Au to p+p changeover during Run-3. The complicated and messy gasket approach was then seen as unnecessary for future trays.

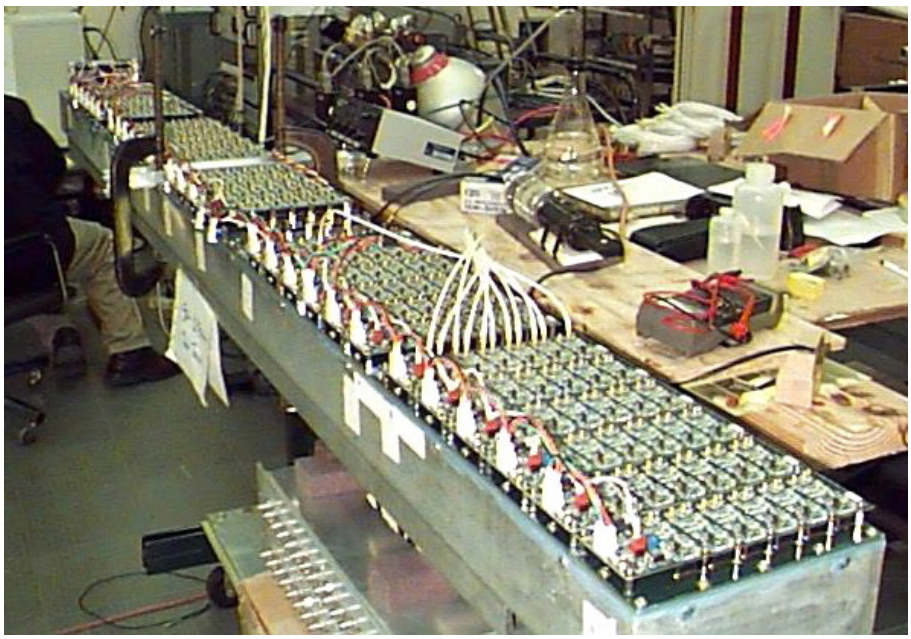


Figure 4: The final TOFr tray under test at Rice.

nation of those used in TOFr in Run-3 (to allow studies of possible aging effects) and new productions from USTC and, for the first time, Tsinghua. Major improvements to the mechanical design were attempted in several areas. These areas included the (hugely labor-intensive) rail assembly fabrication, and the (unimpressive) gasket-based sealing of the electronics to the gas volume. The electronics model was also quite different in philosophy, although the output of the on-board electronics was still intended for a CAMAC-based digitization system.

The welded and tapped rail assembly of TOFr was replaced by a vastly simpler approach for TOFr'. In fact, the rail assembly was removed from the design completely. Instead, a single piece of aluminum, called the "top assembly," was stamped, braked, and welded so that it fit over a TOFr-style bottom assembly in a "shoe box" design. The TOFr' top assembly is shown in Figure 5 and was fabricated completely out-of-house at Oaks Precision. Like the bottom assembly, the interior vertical edges (where the side walls meet) of the top assembly are welded. Joints that were sealed by hand in TOFr then became solid metal (welds at the short edges, braked sheet aluminum for all the long edges).

Another unattractive feature of the TOFr rail assembly was the need to tap $\sim$200 holes to allow the FEE to be mounted (all needing gas sealing). In TOFr', the FEE mount points, and the top assembly to bottom assembly mount points, now involve embedded PEM studs or nuts installed to few-mil precision by machine. Also, the top assembly is now a single piece of (90mil-thick) aluminum, which was mechanically more stable and easier to gas seal overall compared to the conglomeration of hand-machined and welded aluminum angle and plate in the TOFr rail assembly.

The interior of the TOFr' gas box was very similar to that for TOFr. The saw-

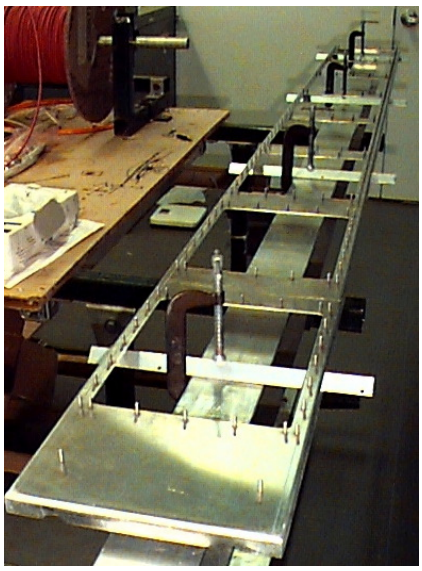


Figure 5: The TOFr' top assembly - a single piece of stamped, braked, and then welded aluminum, with PEM studs for the FEE mounting, and the mounting of this assembly to the MRPC-filled bottom assembly.

tooth approach was again used to hold the MRPCs with respect to the tray bottom assembly. A total of 24 MRPCs were mounted inside the tray on a single HV bus.

Another major difference between TOFr and TOFr' involved mechanical aspects of the on-board electronics. In the interest of working towards the most compact electronics as possible for the full system, the two layers of boards of TOFr (F/T boards + FEE boards) were condensed onto a single layer of electronics called the TFEE boards for TOFr'. This single layer of TFEE boards closed the TOFr' gas volume and produced the large signals needed to go over the long cables to CAMAC. The final TOFr' tray is shown in Figure 6.

The ugly and ineffective gaskets approach for gas-sealing the electronics to the top assembly was removed from the design. For TOFr', the TFEE boards were sealed directly to the top assembly with an adhesive-sealant (24-hour curing time). The choice of this sealant was also improved with respect to TOFr. For this and all subsequent trays we use freon-resistant DC-730 from Dow Corning. We have observed no discoloration or swelling of this sealant in any subsequently-produced trays.

During the initial testing of the completed TOFr' tray it was soon observed that the on-board electronics were very effectively heating the MRPC gas volume. This increased the HV current drawn by the MRPCs and their noise rates by factors of roughly five above those seen in TOFr. An *ad-hoc* cooling loop was thus added at the very end, but due to constraints it was only possible to install this loop in one way, and this way was not very thermally-efficient. This loop can be seen as the 1/2" round aluminum tubing near the outside edge of the TFEE boards in Figure 6. The HV current draw and noise rates remained relatively high when TOFr' ran in

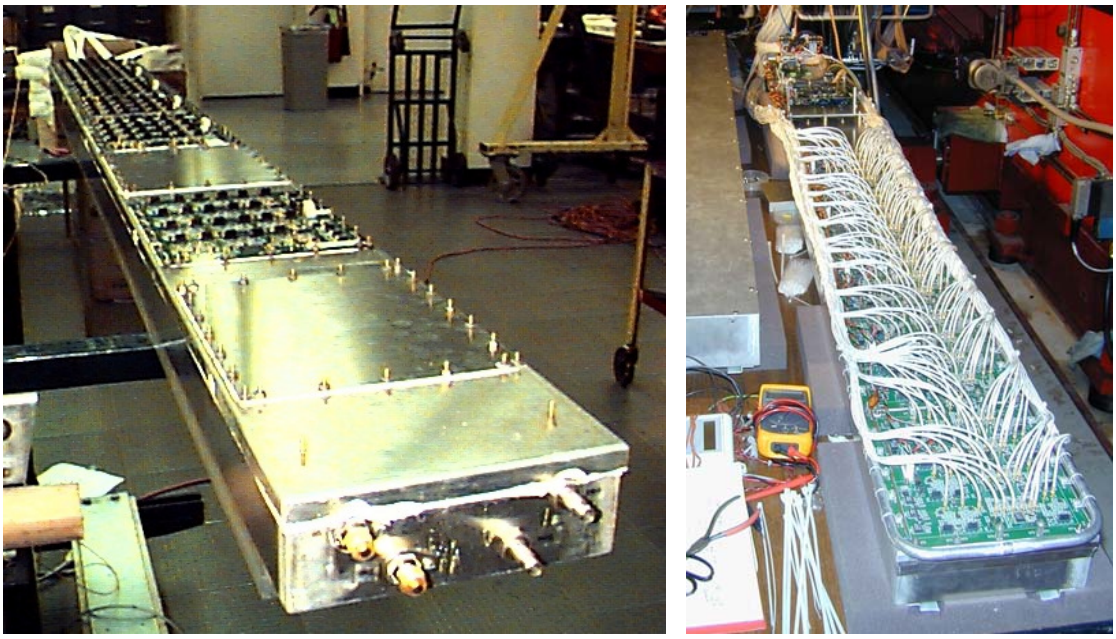


Figure 6: The final TOFr' tray - on the left is the $\eta\sim1$ end just after the closing and sealing of the gas volume, and on the right is TOFr' with all of the electronics and cabling installed just before the tray is to be inserted into STAR.

STAR during Run-4, although the resulting stop-timing resolution obtained was still reasonable (near 100ps).

2.1.3 Run-5 TOFr5 mechanical design

The so-called TOFr5 tray is the third-generation full-sized tray built from the ground-up for the recent Run-5. The MRPCs in TOFr5 are a combination of those used in TOFr in Run-3 and TOFr' in Run-4 (to allow studies of possible aging effects) as well as sixteen newly-produced modules from Tsinghua. The shoe-box style top assembly with PEM-based mount points tried in TOFr' was retained in the TOFr5 design, although significant revisions to this piece were required for this iteration.

On-board time digitization was used for the first time in Run-5. There were two layers of electronics. The layer that closes the gas box, called TAMP for TOFr5, only does the pre-amplification and the input protection and hence does not draw enough power to significantly heat the gas box and the MRPCs. The second layer of electronics, called TDIG for Run-5, discriminates the pre-amplified signals provided by TAMP and feeds the pulse leading edge and trailing edge signals to CERN HPTDC chips for clock-based digitization. While removing the need for kilo-miles of signal cable and full floors of racks for a full CAMAC-based system, this local digitization approach has a number of additional performance advantages. The HPTDC is, however, a large chip that demands a careful stress-free mechanical mounting as well as locally low-temperatures (<60 °C preferred). Thus, TOFr5 also includes a more

tightly-integrated cooling loop.

An outer metal cover to protect these electronics was thus required for the first time. Also, the overall height of the gas volume, the electronics layers and the outer protective layer now needed to shrink to conform to the fact that all 120 of the BEMC modules were installed in STAR prior to Run-5.

Also attempted in TOFr5 was a new approach for holding the MRPCs with respect to the tray body that would be less labor-intensive and of a higher-precision than the sawtooth approach. Dropping the NOMEX as the basic material for the MRPC placement scheme was also a goal, as no-one likes to work fiberglass. Dropping the adhesive from the MRPC positioning scheme would also reduce by 1-2 days the real-time required for this step (for curing).

Pre-tested TAMP boards were sealed to the top of the top assembly again using DC 730 freon-resistant sealant. The cover assembly was then installed over the TAMP layer, and this top+cover assembly was then mounted *on its side* into an MRPC installation jig.

In TOFr and TOFr', the MRPCs are mounted to the long inside walls of the bottom assembly, and the electronics-filled rail or top assembly, respectively, was then mounted onto the filled bottom assembly. TOFr5 replaces the sawtooths approach with one that holds the MRPCs with respect to the top assembly using only two mechanical pieces called 'inner sides'. These are two long and narrow pieces of 1/4"-thick acrylic sheet that sit vertically inside the gas volume just inside the two long and narrow walls of the gas box. Slots are cut into the two inner sides at specific locations and angles, and each of these slots holds one MRPC at an extremely well-defined position with respect to all of the other MRPCs.

Figure 7 shows TOFr5 during the MRPC installation. The top assembly is seen mounted on its side in a specific table jig. First, one inner side (the lower one in this view) is mounted to the "lower brackets" which attach to the underside of the top assembly. The MRPCs are then placed vertically into the slots in this inner side. The installation typically starts at the low-η end and proceeds across the tray from there. The MRPC signal pigtails are connected to the TAMP boards as each MRPC is installed. The HV busses are added later (when the tray is on its back, see below).

Once all the MRPCs are placed into the lower inner side, the other inner side is installed, and the loaded top assembly is then rotated as a whole by 90 degrees so that MRPCs are above and the top assembly is below, resting on the electronics cover.

A view of the high-η end of the tray when it is in such a full-loaded position is shown in figure 8. At this point, a number of important signal connectivity tests can occur during the tray final assembly, which is an improvement over that possible in the TOFr and TOFr' fabrication. In fact, a few MRPC-to-FEE connection problems were located and fixed well before the tray was finally sealed. One signal pigtail broke free from its solder point on an MRPC side, and a few signal pigtail connectors at the TAMP side were incompletely crimped.

Once TOFr5 was to the point seen in figure 8, the final step of the TOFr5 assembly just involved lowering the bottom assembly down onto the loaded top assembly and

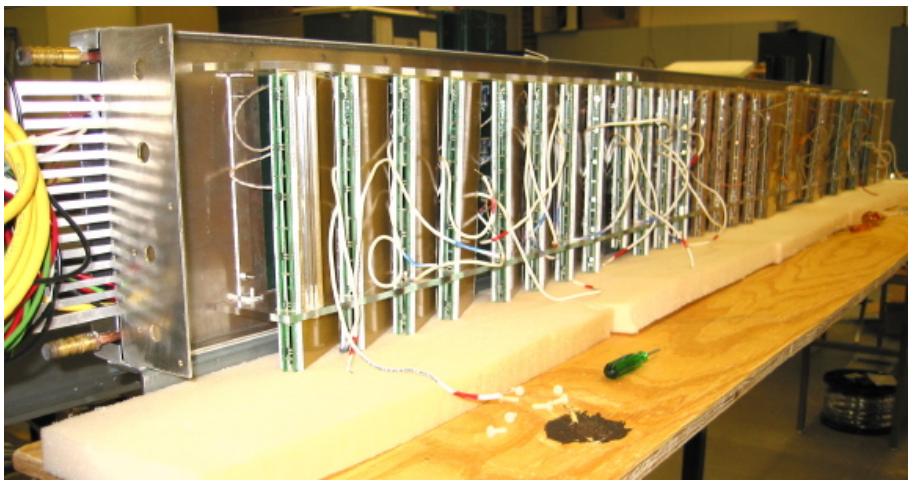


Figure 7: The TOFr5 tray during the module installation into the inner sides.

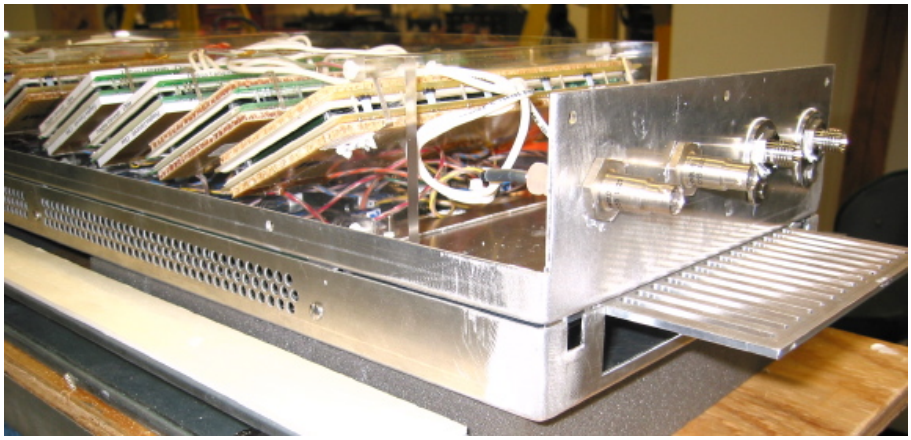


Figure 8: A close-up of the TOFr5 inner sides holding the MRPCs and installed onto the (inverted) top assembly.

sealing this interface. After curing, the completed tray assembly was then be rotated back to 'electronics-up,' the cover assembly was removed, and then gas flow and the next round of tray HV, noise and other tests could proceed.

The Barrel Calorimeter (BEMC) was completely installed during the shutdown just before Run-5. The TOFr5 tray was designed to be the first generation tray that could fit into STAR in the presence of the full BEMC, and it does.

The installation of TOFr5 was made somewhat difficult due to ∼100mils of bowing of the bottom assembly caused by the welding of the tray feet. This bowing will be suppressed in future trays by better jigging at the tray fabrication site (Oaks Precision). If TOFr6 is not significantly improved in this regard, the attachment of the feet will revert to the pop-rivet approach used in TOFr, or an epoxy approach will be used. This results in a few more holes to seal compared to TOFr5 but would

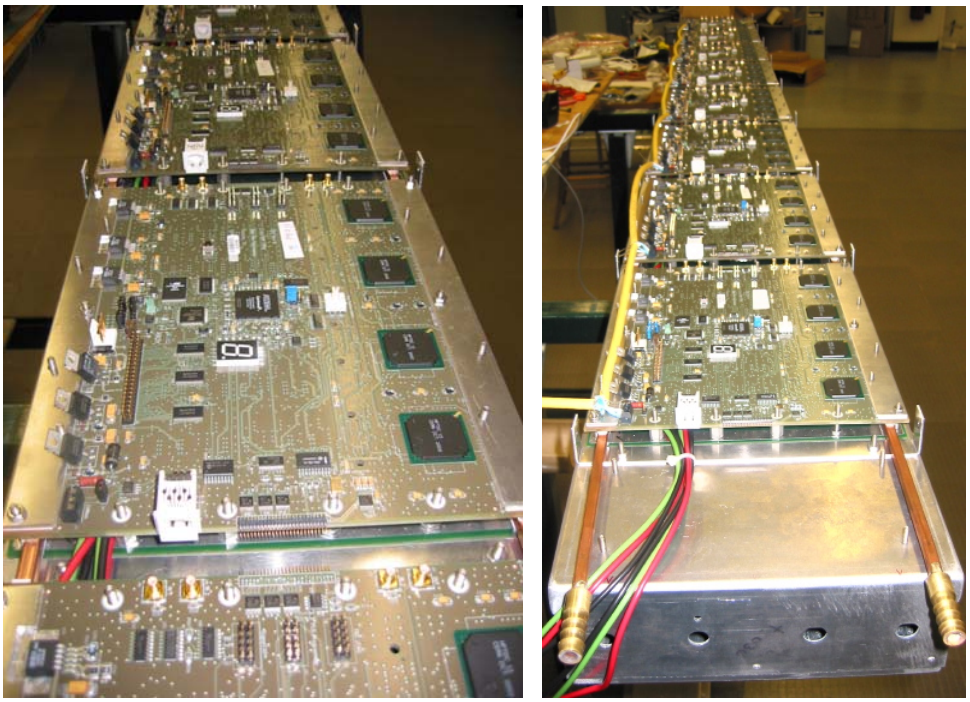


Figure 9: Shown on the left are the upper level of TOFr5 electronics boards called TDIG. The CERN HPTDC chips are the large chips on the right edge of this left-most image. On the right is the TOFr5 tray during an early electronics testing-stage at Rice. The Canbus cable is the yellow one along the left side of this photograph, while the cooling loop in between the TAMP and TDIG layers is seen at the bottom of the image.

address the bowing problem completely. Welded feet are expected to be stronger; this is the preferred approach at this point.

2.1.4 Run-6 TOFr6 mechanical design

The fourth-generation TOFr tray for STAR, "TOFr6," will be produced in the next few months, and at least one of these trays will be installed in STAR for RHIC Run-6. The major improvements to the mechanical design are already completed. The expected design revisions will be small tweaks to improve the ease of final assembly, plus changes to the top assembly required to keep up with the replacement of TOFr5's TAMP boards with TOFr6's TINO boards. These boards are the first layer of FEE and they also seal to the top assembly to close the gas box.

The Inner Sides of TOFr5 were made of ordinary acrylic. While somewhat fragile, there were no problems with the inner sides cracking or breaking during the TOFr5 fabrication. Nonetheless, TOFr6 will use the stronger and more-rigid "Lexan" instead of acrylic.

We have shown that the HPTDC-based TDIG boards satisfy the performance requirements on the start-side. NINO was designed to feed the HPTDC, so we have

Figure 10: The TOFr5 tray with the outer perforated cover installed, shown just before the tray was installed in STAR for Run-5.

always intended to study electronics based on this chip in STAR.[4] We have tested an ALICE-prototype board that uses the NINO chip. The TINO board design is complete and the first prototype boards are in fabrication. TOFr6 will be a full-sized prototype for STAR using both the NINO and HPTDC chips (on TINO and TDIG respectively). At present, we expect that there will be two TOFr6 trays installed for RHIC Run-6.

The concept of an embedded cooling loop in between two layers of electronics used in TOFr5 will be retained in TOFr6, with some slight modifications. We are planning on a rectangular copper loop for the TOFr6 version. This will remove the need to fabricate the various aluminum shims that were needed for TOFr5.

The temperature, power, and heat-flow tests will be performed on the new tray. We will have constructed (at Oaks) both a perforated cover *a la* TOFr5 and a solid cover. This will allow us to investigate the efficiency of the water path and the total radiated power for both cases and to compare them directly. The power flow estimates based on TOFr5 imply that the replacement of the TOFr5 perforated cover with a solid one may reduce the total radiated power by 10-20 W (out of a total of ∼35 W for TOFr5).

[4]The BNL DAC's also explicitly recommended this chip.

2.2 Mechanical design summary

The first TOFr tray showed that the MRPC technology is viable for STAR. The subsequent trays have also worked for PID and STAR physics. The mechanical design of the subsequent full-sized prototypes reduced the manpower and time required to fabricate the tray while also improving key tolerances such as the MRPC positioning. For each generation, it has also been necessary to adapt to new electronics models and cooling schemes. The main differences between the different TOFr generations are summarized in Table I.

2.3 Final Tray Fabrication "Detailed" Procedure

The TOFr5 design differs from what we expect to build for the full system in only trivial ways (screw positioning and so on). Thus, the manpower and procedure needed to produce trays for the full system is now well-understood. This procedure is outlined in this section.

The procedure assumes 1 FTE undergraduate (as two persons, each at the maximum of 20 hours/week), and 1 FTE mechanical technician, over the two year lifetime of the tray assembly and testing project. The procedure needs to be able to produce two trays per week during full production in order to keep pace with the MRPC and Electronics delivery schedules.

The detailed fabrication procedure for a single tray is outlined in Figures 11, and 12. This plan is based entirely on the TOFr5 experience. To scale this plan reasonably to the full project, we make the following additional assumptions.

- We are not space limited. There are four main areas at the tray fabrication site. These are the "Tray Prep" area, the "Tray Assembly" area, the "Tray Testing" area, and the Storage/Shipping area. These spaces are identified and allocated to the project as described later in this subsection.

- There are four trays "in the fabrication system" at any one time. Two trays are in the "Tray Prep" area, and two trays are in the "Tray Assembly" area. At the end of each calender week, the two trays in the Tray Prep area move to the Tray Assembly area, while the two trays in the Tray Assembly area move to the Tray Testing area. At this time, two new trays enter the Tray Prep area. Once trays have been completely tested in the Tray Testing area, they move to the Storage Area to be prepared for shipping to BNL.

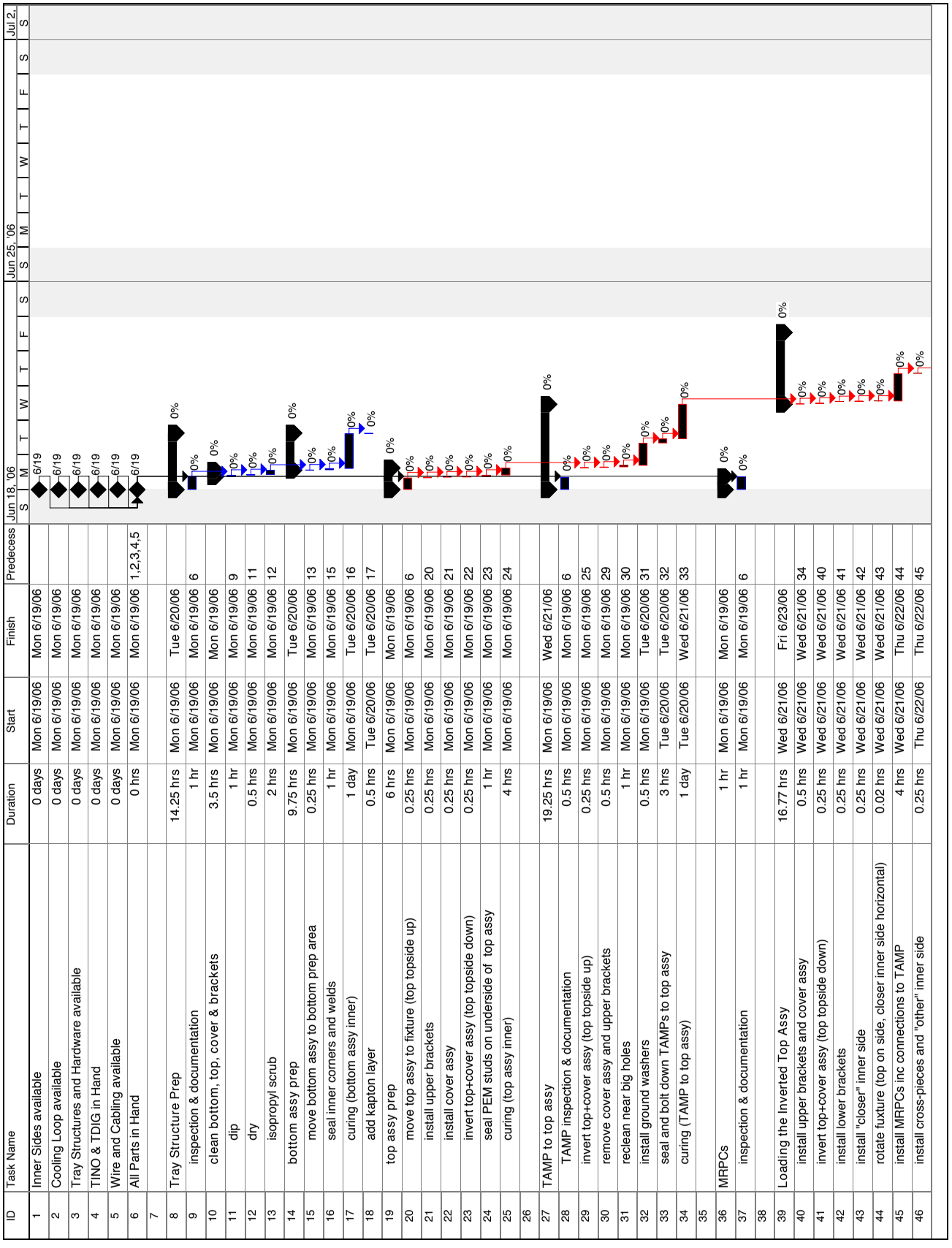
- Machine shop time, such as for the fabrication of the inner sides and the cooling loops, is a contributed resource. The only costs for these components are those for the raw materials and the preparation for installation (cleaning, & QA/QC).

This schedule results in the assembly of two trays per calender week, which matches the assumptions in the overall project plan. One notices that a significant fraction of the time required to fabricate a single tray is spent waiting for adhesive/sealant to cure. There are several of these steps - one for the tray bottom and

Table I: A summary of the design evolution of the various MRPC-based STAR TOFr trays.

Design Area	TOFr (Run-3)	TOFr' (Run-4)	TOFr5 (Run-5)	TOFr6 (Run-6)
Gas box	CTB prototype	custom for Run-4	custom for Run-5	custom for Run-6
Feet attachment	rivets & sealant	plug-welds	plug-welds	improved plug-welds
No. of MRPCs	28	24	32	32
MRPC placement style	sawtooths	sawtooths	acrylic inner sides	lexan inner sides
MRPC placement fab.	by hand on bandsaw	by hand on bandsaw	DXF→Hurco machine	DXF→Hurco machine
MRPC installation	gluing over sev. days	gluing over sev. days	inner sides insertion	inner sides insertion
FEE Style	2 layers, F/T→FEE	1 layer, TFEE	2 layers, TAMP→TDIG	2 layers, TINO→TDIG
FEE mounting	welded rail assy, tapped	single-piece top, PEM	single-piece top, PEM	single-piece top, PEM
MRPC→FEE	6 twisted pairs	6 twisted pairs	6 twisted pairs	two ribbon cables
DAQ model	CAMAC on platform	CAMAC on platform	TDIG on-board	TDIG on-board
R/O model	ethernet	ethernet	SIU/RORC	SIU/RORC
Cooling	none	round Al tubing at edge	embedded sq. Cu tube	embedded rect. Cu tube
Tray total height	∼8”	∼8”	4.5”	4.5”
Outer protective skin	none	none	50-mil Al, perforated	50-mil Al, solid

17



ID	Task Name	Duration	Start	Finish	Predecess
1	Inner Sides available	0 days	Mon 6/19/06	Mon 6/19/06	
2	Cooling Loop available	0 days	Mon 6/19/06	Mon 6/19/06	
3	Tray Structures and Hardware available	0 days	Mon 6/19/06	Mon 6/19/06	
4	TINO & TDIG in Hand	0 days	Mon 6/19/06	Mon 6/19/06	
5	Wire and Cabling available	0 days	Mon 6/19/06	Mon 6/19/06	
6	All Parts in Hand	0 hrs	Mon 6/19/06	Mon 6/19/06	1,2,3,4,5
7					
8	Tray Structure Prep	14.25 hrs	Mon 6/19/06	Tue 6/20/06	
9	inspection & documentation	1 hr	Mon 6/19/06	Mon 6/19/06	6
10	clean bottom, top, cover & brackets	3.5 hrs	Mon 6/19/06	Mon 6/19/06	
11	dip	1 hr	Mon 6/19/06	Mon 6/19/06	9
12	dry	0.5 hrs	Mon 6/19/06	Mon 6/19/06	11
13	isopropyl scrub	2 hrs	Mon 6/19/06	Mon 6/19/06	12
14	bottom assy prep	9.75 hrs	Mon 6/19/06	Tue 6/20/06	
15	move bottom assy to bottom prep area	0.25 hrs	Mon 6/19/06	Mon 6/19/06	13
16	seal inner corners and welds	1 hr	Mon 6/19/06	Mon 6/19/06	15
17	curing (bottom assy inner)	1 day	Mon 6/19/06	Tue 6/20/06	16
18	add kapton layer	0.5 hrs	Tue 6/20/06	Tue 6/20/06	17
19	top assy prep	6 hrs	Mon 6/19/06	Mon 6/19/06	
20	move top assy to fixture (top topside up)	0.25 hrs	Mon 6/19/06	Mon 6/19/06	6
21	install upper brackets	0.25 hrs	Mon 6/19/06	Mon 6/19/06	20
22	install cover assy	0.25 hrs	Mon 6/19/06	Mon 6/19/06	21
23	invert top+cover assy (top topside down)	0.25 hrs	Mon 6/19/06	Mon 6/19/06	22
24	seal PEM studs on underside of top assy	1 hr	Mon 6/19/06	Mon 6/19/06	23
25	curing (top assy inner)	4 hrs	Mon 6/19/06	Mon 6/19/06	24
26					
27	TAMP to top assy	19.25 hrs	Mon 6/19/06	Wed 6/21/06	
28	TAMP inspection & documentation	0.5 hrs	Mon 6/19/06	Mon 6/19/06	6
29	invert top+cover assy (top topside up)	0.25 hrs	Mon 6/19/06	Mon 6/19/06	25
30	remove cover assy and upper brackets	0.5 hrs	Mon 6/19/06	Mon 6/19/06	29
31	reclean near big holes	1 hr	Mon 6/19/06	Mon 6/19/06	30
32	install ground washers	0.5 hrs	Mon 6/19/06	Tue 6/20/06	31
33	seal and bolt down TAMPs to top assy	3 hrs	Tue 6/20/06	Tue 6/20/06	32
34	curing (TAMP to top assy)	1 day	Tue 6/20/06	Wed 6/21/06	33
35					
36	MRPCs	1 hr	Mon 6/19/06	Mon 6/19/06	
37	inspection & documentation	1 hr	Mon 6/19/06	Mon 6/19/06	6
38					
39	Loading the Inverted Top Assy	16.77 hrs	Wed 6/21/06	Fri 6/23/06	
40	install upper brackets and cover assy	0.5 hrs	Wed 6/21/06	Wed 6/21/06	34
41	invert top+cover assy (top topside down)	0.25 hrs	Wed 6/21/06	Wed 6/21/06	40
42	install lower brackets	0.25 hrs	Wed 6/21/06	Wed 6/21/06	41
43	install "closer" inner side	0.25 hrs	Wed 6/21/06	Wed 6/21/06	42
44	rotate fuxture (top on side, closer inner side horizontal)	0.02 hrs	Wed 6/21/06	Wed 6/21/06	43
45	install MRPCs inc connections to TAMP	4 hrs	Wed 6/21/06	Thu 6/22/06	44
46	install cross-pieces and "other" inner side	0.25 hrs	Thu 6/22/06	Thu 6/22/06	45

Figure 11: Page one of the detailed schedule for tray assembly.

ID	Task Name	Duration	Start	Finish	Predecess
47	rotate fixture (top topside down)	0.25 hrs	Thu 6/22/06	Thu 6/22/06	46
48	install reynolds connectors with sealant	0.5 hrs	Thu 6/22/06	Thu 6/22/06	47
49	install HV bus wiring to each MRPC	2 hrs	Fri 6/23/06	Fri 6/23/06	48
50	install gas feedthroughs & interior tubing	0.5 hrs	Thu 6/22/06	Thu 6/22/06	47
51	curing (F/T connectors on top assy)	2 hrs	Thu 6/22/06	Thu 6/22/06	48,50
52	HV tests	2 hrs	Thu 6/22/06	Thu 6/22/06	51
53	MRPC connectivity tests	6 hrs	Thu 6/22/06	Fri 6/23/06	51
54					
55	Tray Closing	9.5 hrs	Fri 6/23/06	Mon 6/26/06	
56	test fit bottom assy onto top assy	0.25 hrs	Fri 6/23/06	Fri 6/23/06	53
57	scribe	0.25 hrs	Fri 6/23/06	Fri 6/23/06	56
58	remove bottom assy and apply sealant	0.5 hrs	Fri 6/23/06	Fri 6/23/06	57
59	install bottom assy, install machine screws	0.5 hrs	Fri 6/23/06	Fri 6/23/06	58
60	curing (bottom assy onto top assy)	1 day	Fri 6/23/06	Mon 6/26/06	59
61					
62	Tray Closed	0 hrs	Mon 6/26/06	Mon 6/26/06	60
63					
64	Electronics installation and Testing	32.25 hrs	Mon 6/26/06	Fri 6/30/06	
65	rotate tray (top topside up)	0.25 hrs	Mon 6/26/06	Mon 6/26/06	62
66	move completed tray to tray test area	0.5 hrs	Mon 6/26/06	Mon 6/26/06	65
67	Gas flow for testing	8.25 hrs	Mon 6/26/06	Tue 6/27/06	
68	connect tray to gas system	0.25 hrs	Mon 6/26/06	Mon 6/26/06	66
69	gas flow started	1 day	Mon 6/26/06	Tue 6/27/06	68
70	Gas Leak testing wtih sniffer	1 day	Mon 6/26/06	Tue 6/27/06	68
71	Gas Quality Acceptable for HV tests	0 hrs	Tue 6/27/06	Tue 6/27/06	69
72	TDIG Installation	17.5 hrs	Mon 6/26/06	Wed 6/28/06	
73	remove cover assy and upper brackets	0.5 hrs	Mon 6/26/06	Tue 6/27/06	65
74	install cooling loop	0.5 hrs	Tue 6/27/06	Tue 6/27/06	73
75	install TDIG boards	2 hrs	Tue 6/27/06	Tue 6/27/06	74
76	install LV bus (lugs on-tray to boards)	1 hr	Tue 6/27/06	Tue 6/27/06	75
77	Install TDIG cabling (canbus etc)	2 hrs	Wed 6/28/06	Wed 6/28/06	81
78	LV power test	1.5 hrs	Wed 6/28/06	Wed 6/28/06	
79	install LV test cables (supply to lugs on-tray)	0.5 hrs	Wed 6/28/06	Wed 6/28/06	76
80	LV power-up and documentation	1 hr	Wed 6/28/06	Wed 6/28/06	79
81	LV test passed	0 hrs	Wed 6/28/06	Wed 6/28/06	80
82	Firmware and other electronics setup	2 hrs	Wed 6/28/06	Wed 6/28/06	77,81
83	HV Performance	4.25 hrs	Tue 6/27/06	Wed 6/28/06	
84	connect HV cables	0.25 hrs	Tue 6/27/06	Tue 6/27/06	71
85	ramp HV and collect V/I data	4 hrs	Tue 6/27/06	Wed 6/28/06	84
86	Tray Stable at Full Voltage	0 days	Wed 6/28/06	Wed 6/28/06	85
87	DAQ Performance	18 hrs	Wed 6/28/06	Fri 6/30/06	
88	Noise rate tests, dead channel identification	2 days	Wed 6/28/06	Fri 6/30/06	86
89	INL Calibration	1 day	Thu 6/29/06	Thu 6/29/06	82
90	Final test documentation	0 hrs	Fri 6/30/06	Fri 6/30/06	88,89
91					
92	Tray complete & Ready for Cosmics Testing	0 hrs	Fri 6/30/06	Fri 6/30/06	90

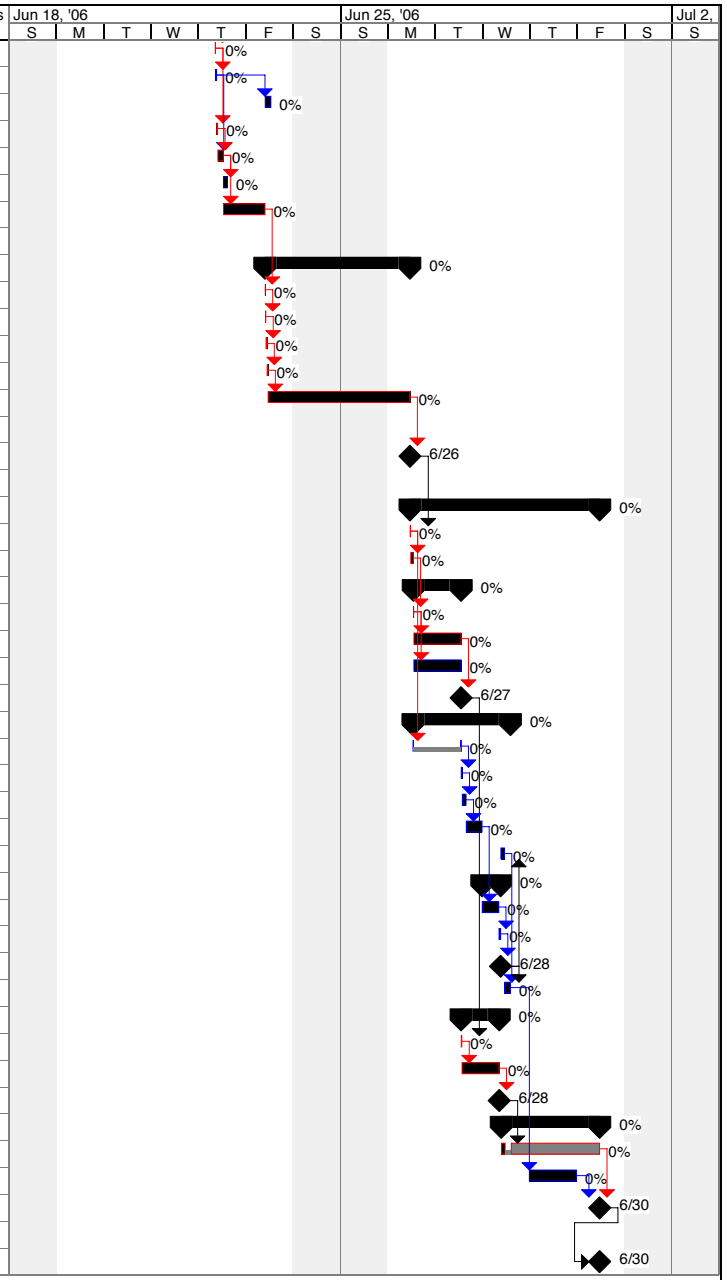


Figure 12: Page two of the detailed schedule for tray assembly.

top preparation, one for the sealing of the TINO boards to the top, and one for the sealing of the bottom onto the (MRPC-filled) top. It is this fact that allows four trays to be in the fabrication system at any one time. While one unit is curing in either the Tray Prep or Tray Assembly areas, the available manpower can move over to work on other units.

Thus the time intervals required for each step in Figures 11 and 12 are all increased by a factor of two with respect to the TOFr5 experience. This thus accounts for the fact that two trays are under construction in both the Prep and Assembly areas at any one time.

2.4 Final Tray Fabrication

In this subsection, the details on the available floor space at the fabrication sites and the necessary fabrication fixtures are described. The fabrication sites are Rice and UT-Austin. The former concentrates on the tray body hardware (bottom, top, and cover assemblies) and the electronics. The latter receives the tray hardware and electronics from Rice, MRPCs from USTC and Tsinghua, and then concentrates on the final assembly and testing of full trays.

A structure such as that shown in Fig. 15 is needed at Rice for the initial tray QA. This structure can be moved to UT-Austin once the trays are delivered there.

The space available at Rice is shown in Figure 13. The areas shaded in blue are allocated to this project and are sufficient. The space available at UT-Austin is shown in Figure 14. According the the discussion in the previous subsection, we following assignments have been made.

- Tray Preparation Area: **RLM 3rd level**.
- Tray Assembly Area: **RLM 10.318**.
- Tray Testing Area: **RLM 10.306**.
- Storage Areas: **RLM 10.318A** (for components needed for tray fabrication such as MRPCs, electronics, cooling loops, inner sides, etc.), and the **ENS Building, Physics Lab** (for storage of fully fabricated and tested trays, and preparation for shipping to BNL).

These areas, the jigs required to meet the production schedule, are now described.

2.4.1 Tray Preparation Area

The trays structures produced at Oaks Precision in Houston are first delivered to Rice. Here they are checked for tolerances and documented. The trays are then shipped to UT-Austin, where they are stored until needed. The trays enter the fabrication stream at UT-Austin in the Tray Preparation area. Here the following tasks are performed.

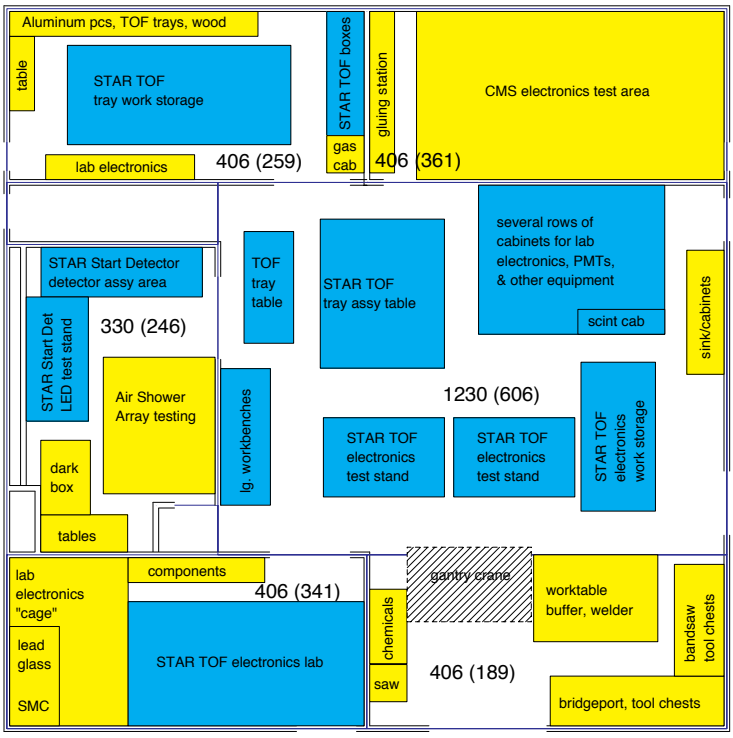


Figure 13: The floor plan of the space available at Rice for the tray box production and QA, as well as the electronics fabrication and testing. The areas dedicated to this project are shown as the blue boxes.

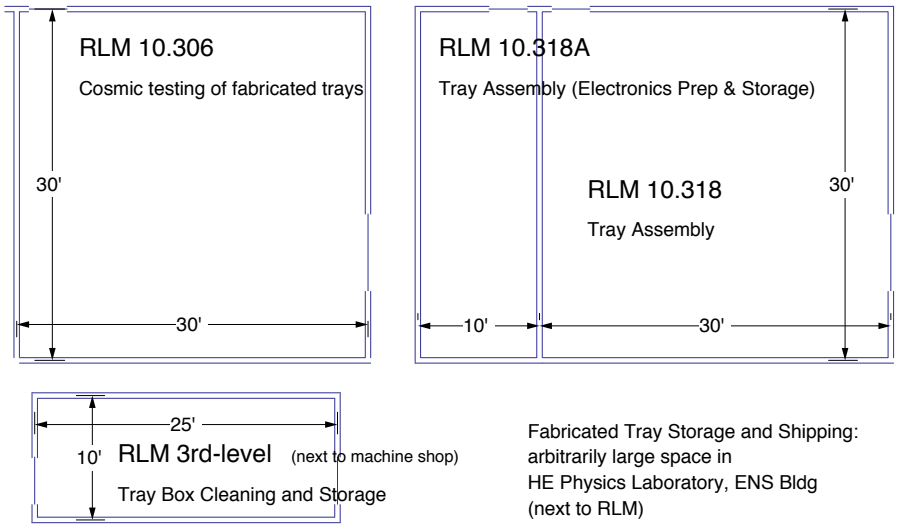


Figure 14: The floor plan of the space available at UT-Austin for the tray final assembly and cosmics testing.

- Tray mechanical structures are thoroughly cleaned.
- Bottom assembly is sealed, and Kapton layer is applied.
- PEM studs in the Top assembly are sealed.
- Components emerging from the UT-Austin machine shop (inner sides and cooling loops) are cleaned and then undergo QA/QC and documentation.

Following these tasks, the tray mechanical components move the the Tray Assembly area.

2.4.2 Tray Assembly Area

In this area the MRPCs, electronics, and mechanical components come together to form complete TOF trays. This assembly process requires two custom tables that are shown in 16. These tables include a pivoting "long-L" which holds the top assembly either on its side (for MRPC installation) or on its back, for testing and all other operations before final sealing.

In this area, the following tasks are performed.

- Sealing of TAMP/TINO electronics into the top assembly.
- Mounting of inverted top+electronics assembly onto a table.
- Installation of inner sides, MRPCs, and the HV bus.
- Open tray testing of the HV bus and the MRPC-to-electronics signal connections.
- Installation and sealing of inverted bottom assembly onto inverted top assembly.
- Installation of the LV bus, TDIG electronics, and cabling.

Following these tasks, the fully loaded TOF trays move the the Tray Testing area.

2.4.3 Tray Testing Area

A completed trays may remain in this are for several weeks. Thus, a large structure for holding many trays (each with all of their gas, power, signal, and control cabling) at once is needed. This structure can be something like that shown in Fig. 15.

The tasks performed in this area are the following.

- Gas flow and leak testing.
- Firmware set-up and TDIG communication tests.
- INL calibrations and documentation for each TDIG board.

- Tray HV stability and current draw tests.
- MRPC noise rate tests for each of the 192 channels.
- Cosmics testing using CTB trays or delay-line chambers as trigger detectors, to allow "real" data to flow throughout the system.

2.4.4 Tray Storage and Shipping Area

Trays that have met all qualification tests in the Tray Testing area are then moved to the storage area. The tasks performed in this area are the following.

- Basic storage of completed trays.
- Packing of completed trays into shipping boxes.

The trays are then shipped to BNL. Once they arrive, they are retested for gas box integrity, HV current draw, and noise rates in each MRPC channel. Once final-qualified and documented, the trays are ready for installation during the next summer shutdown.

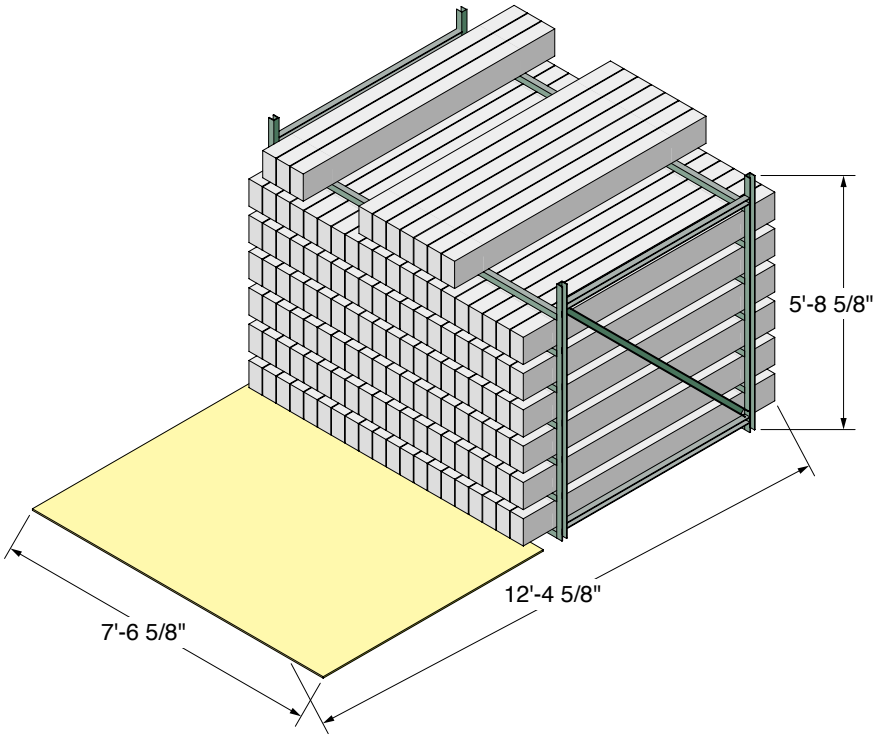


Figure 15: A schematic view of the space required to store 130 trays at any stage of construction.

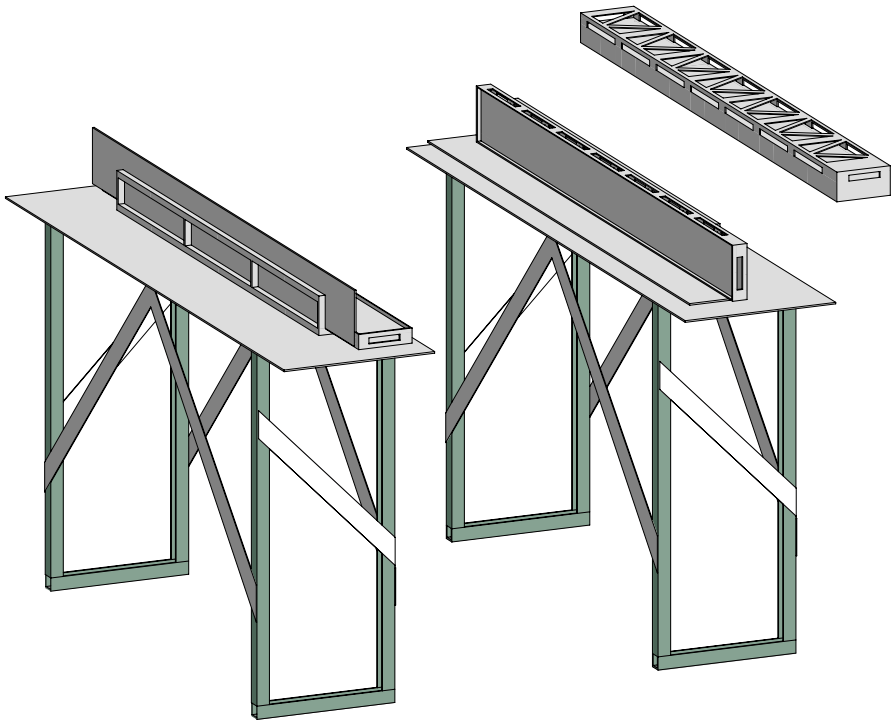


Figure 16: A schematic view of the two tray assembly tables.

3 TOFr5 Power, Temperature, and Heat-Flow Tests

The on-board electronics for TOFr5 draw ∼140W, implying a full system (120 trays) of this design would add ∼17 kW of heat into the very tight cylindrical space between the STAR TPC and BEMC systems. This heat must be removed from inside the pole tips as efficiently as possible in order to limit side-effects in the neighboring subsystems. Radio-frequency (and mechanical) shielding for the TOFr5 electronics using an outer aluminum skin is necessary, and such a skin retains heat at the electronics. The HPTDC chips begin to fail to operate sensibly if their local temperature reaches ∼60 °C. Efficient metallic thermal paths between the ground planes of the electronics and the aluminum mechanical structure of TOFr5 imply some heating of the MRPC gas box, which is known from Run-4 to significantly increase MRPC noise rates and current draw.

The actual magnitude of all of these effects for the final configuration of "final" TAMP and TDIG boards (8 each), mounted on the final mechanical structure (gas box, plus mechanical support for all MRPCs, electronics, and outer cover) for Run-5, and powered up, were thus of special interest. A "System Test" of the final components of TOFr5 was performed in order to investigate these power, heat flow, and temperature issues, and the results are described below. The following is an abbreviated version of the more detailed write-up of Ref. [4].

3.1 Equipment

The TOFr5 electronics layout has two layers of circuit boards, where the first layer has comparatively few components. This first layer, the TAMP layer, closes the gas box and provides pre-amplified and input-protected MRPC signals to a second layer of TDIG boards which do the discrimination, digitization, trigger matching, hit counting, and data buffering. Compared to TOFr' (Run-4), the TOFr5 design includes a tightly-integrated water path that uses square 1/4" copper tubing that runs along the two long lengths of the tray and between the two layers of electronics boards. A view of the $\eta\sim1$ end of the TOFr5 tray, cooling loop, and electronics at an intermediate stage of the TOFr5 fabrication is shown in figure 17.

The vertical gap between the TAMP and TDIG layers is set by connectors at 7/16". The cooling loop is 1/4"-thick, leaving 3/16" which is made up of two aluminum pieces (1/8" and 0.05") and thermally conductive plastic shims (7 and 11 mils). The hope was that this water to electronics thermal path would be efficient enough to bring the majority of the electronics' total power out of the STAR pole tips via water and hence keep the local temperatures comfortably low. We tested the efficiency of this path with the set-up shown in figures 18 and 19.

The water source was Rice tap water, available at the faucet at ∼2.3 Gpm and 31 °C. Approximately 10' of 1/2" vinyl braided hose brings the water to a heat exchanger (an ice cooler holding 40' of coiled 3/8" Copper tubing), then ∼30' of hose connects to the input of tray cooling loop, and ∼40' of hose returns the water. The flow rate through the heat exchanger and the 30' hose was 2.2 Gpm, while the (more relevant)

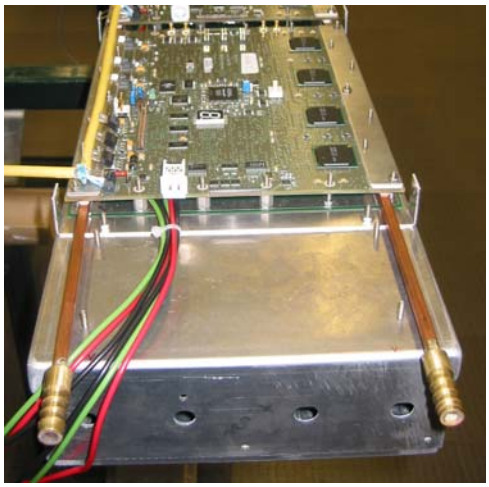


Figure 17: End view of the TOFr5 tray at an intermediate stage of the fabrication. The top layer of electronics are the TDIG boards. The square copper cooling loop is just under the TDIG layer, and just under the cooling loop is the TAMP layer which closes the gas box.

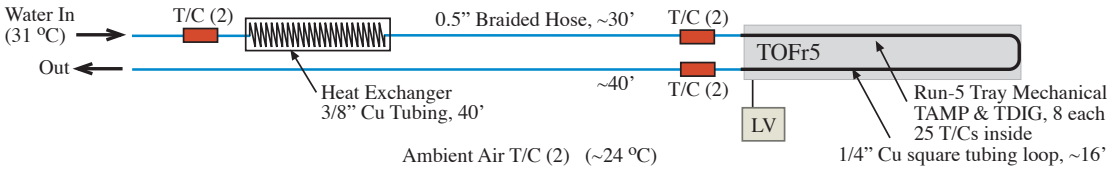


Figure 18: Schematic view of the equipment for these tests.

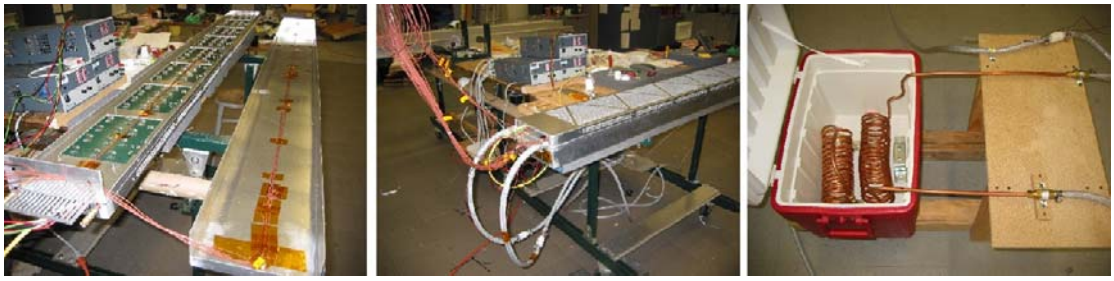


Figure 19: Shown on the left is the TOFr5 bottom and top assemblies and the thermocouple wiring for the interior of the gas box. In the center, TOFr5 reassembled and running during these tests, and on the right is the heat exchanger.

flow rate through the entire system was 1.36 Gpm. The water flow rate in STAR is locally adjustable in the range from ∼0.5 to 2 Gpm.

The full complement of TAMP and TDIG pairs (8 pairs) was installed on the final TOFr5 tray structure [5]. Low voltage for these electronics was provided by the Kepco supplies to be used in Run-5. The low voltages, currents, and total electrical power for TOFr5 are summarized in Table II.

Table II: TOFr5 low voltages, currents, and electrical power estimates.

V (Volts)	I (Amps)	P (Watts)
+4.2	16	67
+4.2	11	46
-8.5	3	26
(total)		139±10

The temperatures at a number of locations inside the tray and the electronics volume are obtained from a Kinetics Systems 1992 Thermocouple Termination Panel and a 3516 Scanning A/D [6]. The total number of temperature measurements is 32, one of which is internal to the 1992 (the "reference temperature"). The remaining 31 channels read remote temperatures over type TT thermocouple wire. The Kinetics units are read-out via CAMAC over a GPIB interface to a PC with a custom DAQ code. This code reads all 32 temperatures continuously with a 4 second interval between reads, and stores each 32-channel read with a time stamp to an ntuple which is analyzed in ROOT. The thermocouple locations on-tray, on the ambient air, and in the water path, are summarized in Table III. The calibration of the data from thermocouple system and the resulting temperature resolutions in °C following these calibrations is discussed in section 3.2 below.

Table III: The thermocouple locations for the present tests.

T/C	Location	T/C	Location
0	Reference Inside KS1992	16	TDIG Regulator pos6
1	Tray Inside Air $\eta\sim0.2$	17	TDIG pcb near sensor pos4
2	Tray Inside Air $\eta\sim0.5$	18	TDIG pcb near sensor pos4
3	Tray Inside Air $\eta\sim0.8$	19	Air Gap Above TDIG pos1
4	Tray Side Wall Inner $\eta\sim0.2$	20	Air Gap Above TDIG pos4
5	Tray Side Wall Inner $\eta\sim0.2$	21	Air Gap Above TDIG pos6
6	Under TAMP near sensor pos4	22	TDIG pcb top pos0
7	Under TAMP near sensor pos4	23	TDIG pcb top pos7
8	Air Gap Below TDIG pos1	24	Lab Room Temperature
9	Air Gap Below TDIG pos4	25	Lab Room Temperature
10	Air Gap Below TDIG pos6	26	Water At Tray Input
11	HPTDC1 Chip pos6	27	Water At Tray Input
12	HPTDC4 Chip pos6	28	Water At Tray Output
13	HPTDC2 Chip pos6	29	Water At Tray Output
14	HPTDC3 Chip pos6	30	Water In
15	TDIG Altera Chip pos6	31	Water In

3.2 Temperature Calibrations

A simple calibration of the thermocouple system is required. The first step is the correction for the so-called reference temperature. The second step takes care of channel-dependent offsets in the 1992+3516 system. The details on these calibrations are presented in Ref. [4].

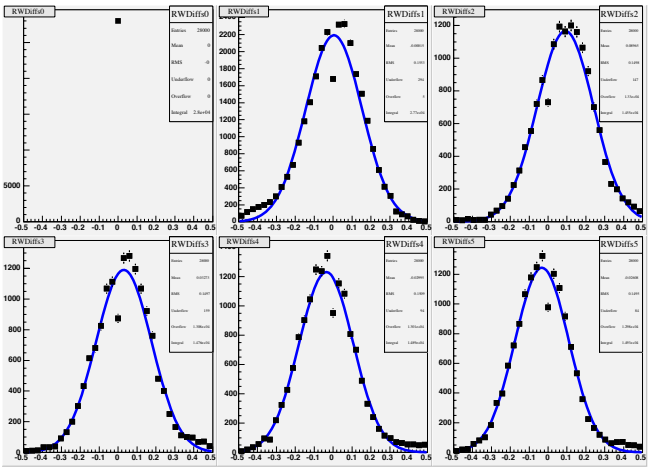


Figure 20: The temperature difference resolution following the calibrations.

The single-channel resolution of the system is indicated in figure 20. Shown in each frame is the difference between a water or ambient air temperature and the first ambient air temperature, *i.e.* frame i shows t$[i+24]-$t$[24]$ where $0 \leq i \leq 5$. The standard deviation of these difference Gaussians is 0.13-0.15 °C, implying a single-channel resolution in single DAQ reads of approximately 0.14*sqrt(2)∼0.2 °C. A typical calculation of an average temperature for some thermocouple at some point during the data-taking involves no less that 15 reads (∼1 minute of real time) so the statistical uncertainty on one-minute averages is ∼0.2/sqrt(15)∼0.06°C. We see slight drifts in the temperatures beyond that expected after the calibrations that are of order 0.02 °C (seen in section 3.4 below). The present calibration scheme could be augmented to suppress this drift, but since the drift is so small in magnitude we choose to simply assign this as systematic error. The total single-channel resolution in single reads is thus estimated to be $0.2 \oplus 0.02 = 0.2$ °C, while the total resolution on one-minute averages of single channels is $0.06 \oplus 0.02 = 0.063$ °C. The total resolution on the difference of two two-channel averages is the same as the total single-channel resolution, or 0.2 °C for single reads and 0.063 °C for one-minute averages. Certain estimates made in section 3.4 are based on averages of this difference of single-read averages over a few hundred reads, for which the total error is taken to be the 0.02 °C systematic error.

3.3 Temperature Asymptotes

These tests consist of a number of different phases, each with a specific configuration of the system (LV on or off, water flow on or off, and so on). Each phase was generally run long enough for asymptotic temperatures to be reached. A graphic depiction of the entire ∼two day experiment is shown in figure 21. The various phases are marked by the different colors and correspond to the configurations shown in the accompanying table.

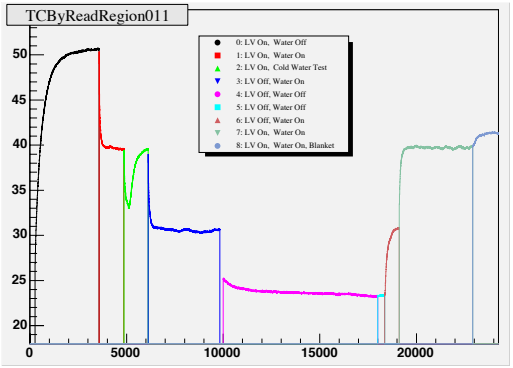


Figure 21: A single temperature in the tray vs. the read number.

Phase	Configuration
0	LV On, Water Off
1	LV On, Water On (31 °C)
2	LV On, Water On (colder)
3	LV Off, Water On
4	LV Off, Water Off
5	LV Off, Water Off
6	LV Off, Water On
7	LV On, Water On
8	LV On, Water On, Blanket

Figure 22: The different data-taking phases.

The asymptotic temperatures reached in the various phases of the data-taking are depicted in figure 23. The black points (phase 0) correspond to no water cooling and indicate the highest temperature reached in the system is ∼53 °C at a LV regulator on the TDIG boards. The temperatures reached on the casing of the TDIG chips themselves is ∼48 °C for the very-high-resolution HPTDCs (stops data), and ∼45 °C for the high-resolution HPTDC (ToT data). The tray interior (inside the gas box) reaches ∼38 °C, while the air gap between the TAMP and TDIG layers reaches ∼45 °C.

These asymptotic temperatures without water cooling are comfortably below the specified maximum levels of 60 °C for the HPTDC chip temperature and 80 °C for the TDIG regulator temperature. Thus, the TOFr5 system should operate correctly in the absence of cooling water. However, water cooling would still minimize the heat radiated into neighboring detectors, minimize the MRPC noise rates, and maximize the service lifetime of the electronics.

Flowing water is seen to reduce the TOFr5 temperatures dramatically. This is seen as the red squares and green triangles (phases 1, 2, and 7), which depict temperatures that are 10-15 °C lower than when water is not flowing (black points, phase 0).

The input water temperature in these tests was 31 °C, while the temperature of STAR 'chilled water' is ∼24 °C. Phase 2 thus includes the operation of the heat exchanger by filling it with ice. That the asymptotic temperatures in this phase are very similar to those at the end of phase 1 simply indicates that phase 2 was ended at a point when all the ice in the heat exchanger had melted and the tray input water temperature was back to that of the water as it comes out of the wall. Estimates for

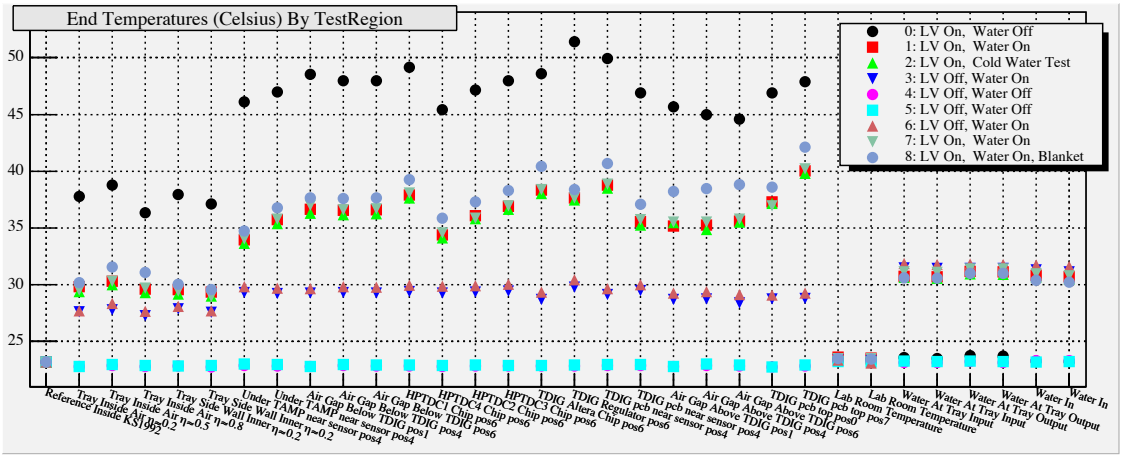


Figure 23: The asymptotic temperatures reached in the various phases of the data-taking.

the temperatures that would have been reached if the cooling water would have been kept at ∼24 °C indefinitely, as in STAR, are thus not shown in figure 23 (but are estimated as described in section 3.5 below).

Phase 8 is similar to phases 1 and 7 in that both LV and 31 °C water flow were on, but includes a covering of the perforated aluminum cover layer on TOFr5 with several layers of plastic wrap and a blanket. This phase was done with the hope of estimating the amount of power being radiated through the perforated aluminum cover. With the perforated cover blocked off, the TOFr5 temperatures reach asymptotic values that are 2-4 °C higher then when the cover is not blocked.

3.4 Power Estimates

The TOFr5 electronics draw 140±10 W per tray. The central goal of the present tests is an estimate of the fraction of this total power that is removed by the water path. The remainder would be radiated into the STAR TPC and BEMC. In this section, we estimate how this 140 W/tray of total TOFr5 power is shared among the possible heat removal mechanisms - water flow in the TOFr5 geometry, radiation, and convection.

The power removed by the water path is a function solely of the flow rate and the difference between the tray output and input water temperatures, according to

$$P_{water}\ (\text{Watts}) = 1.15\ *\ FlowRate\ (\text{liters/hr})\ *\ \Delta T\ (^{\circ}\text{C}). \qquad (1)$$

For the 1.36 Gpm flow rate used in the present tests, this equation becomes

$$P_{water}\ (\text{Watts}) = 355\ *\ \Delta T\ (^{\circ}\text{C}). \qquad (2)$$

The two pairs of thermocouples at the tray water input and output are averaged separately in each read, and the difference between these two averages (output−input) is plotted versus the read number over the entire running period in figure 24.

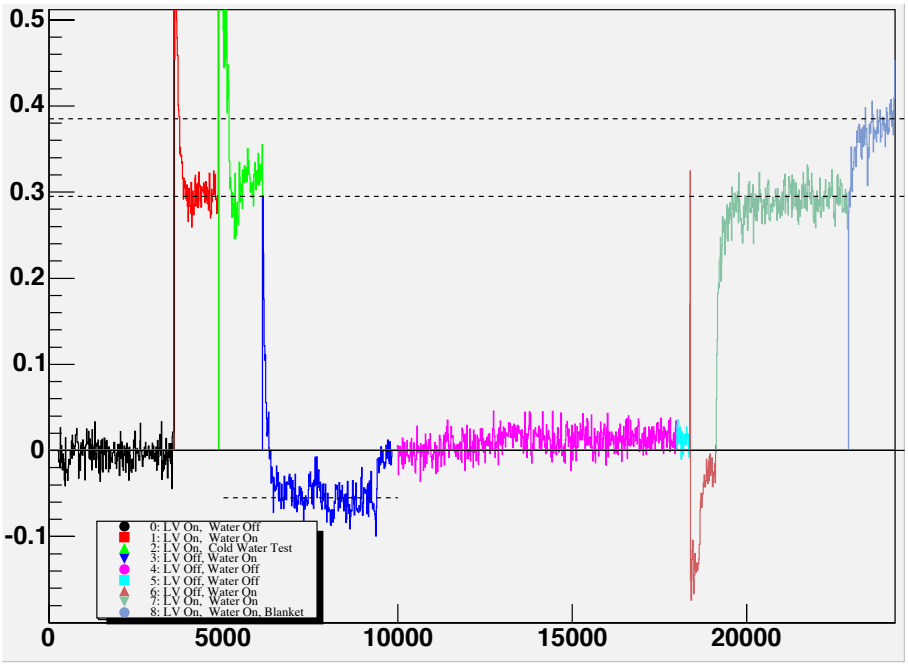


Figure 24: The average output water temperature, (t[28]+t[29])/2 after the calibrations, minus the average input water temperature, (t[26]+t[27])/2, versus the read number (4s/read).

In phase 0, water is not flowing, so the average water temperature difference, output−input, (black points) remains consistent with zero throughout this phase, as expected given the KS1992+3516 offset calibration. The initiation of the (31 °C) water flow at the beginning of phase 1 (red points) causes a dramatic drop in the on-tray temperatures and an increase in the water temperature difference (tray output−input) of ∼0.295±0.02 °C. This implies that the power removed via the 31 °C water path in phase 1 was 105 W, which is ∼75% of the total power dropped by the electronics (140±10 W). This configuration was retested in phase 7, and the water temperature increase observed in this phase is consistent with that observed in phase 1.

Thus, 31 °C water flow removes 3/4 of the total power, and the remaining 1/4 of the total power is carried away radiatively or convectively. This is tested in phase 8, where the plastic wrap and blanket wrapping outside of the TOFr5 tray strongly suppresses both the radiative and convective heat removal paths. In this phase, the asymptotic water temperature difference was observed to be 0.385 ±0.02 °C. The total power being carried away by the water path is thus 136W, which is consistent with 100% of the 140W total power being dropped by the electronics. This result implies that the efficiency of the water path is not limited by its design, but rather by the fact that heat removal via the water flow is competing with radiative and convective heat loss mechanisms at the same time.

The total radiative and convective heat loss of $355 * (0.385 - 0.295) = 32 \pm 7$ W is

made up of the following pieces.

- radiative heat loss from outer aluminum skin of the tray, including the bottom assembly, the outer edges of the top assembly, and the perforated cover. All are aluminum with thicknesses are 0.05", 0.09", 0.063", respectively. The cover is perforated with 0.2" diameter holes on a 60-degree grid with a hole area fraction of 50%,
- radiative heat loss from the TDIG boards (and components on the top of TDIG) through the perforation holes in the cover,
- convective heat loss by room air (unforced and no drafts) flowing in and then out of the perforation holes in the cover.

We now attempt to estimate the relative importance these three mechanisms to provide a full accounting of the total TOFr5 power.

We can dispense with the convective process immediately. The room air was "calm"; it was not being forced across the tray in any way. The power removed by air flow is given by,

$$P_{airflow}\ (\text{Watts}) = 0.125\ *\ FlowRate\ (\text{CFM})\ *\ \Delta T\ (^{\circ}\text{C}). \tag{3}$$

As the air flow rate through the cover, over TDIG boards, then out the cover again could not be larger than 0.1 CFM at any time during the present tests, the heat removed through the cover by convective air flow can not exceed a fraction of one Watt.

We thus assume we are left with only the two radiative processes. We can check that this assumption with the phase 3 results. In this phase, the electronics are unpowered but 31 °C water is still flowing. Here the temperature rise is negative, as in this phase the tray is serving as a "radiator" and removing heat from the water, rather than in phases 1, 2, 7, and 8 where the water is removing heat from the tray. While the distribution of heat sources over and inside the tray is different in these two cases (all local heat generated on the electronics versus all local heat generated on the cooling loop), the efficient all-metal paths between the electronics and the water loop implies that the data from phase 2 should lead to an approximate but direct estimate of the total radiative heat loss. In this phase, the observed water temperature difference is -0.06 °C, which corresponds to 20±7 W. This is not so far off from 32±7 W but again there are caveats for this comparison. We note for fun that a more dramatic example of the tray acting as a radiator to remove heat from the water is seen at the beginning of phase 6. In this case the entire tray is at room temperature. At the initiation of the 31 °C water flow, the water temperature difference (output−input) is ∼-0.14 °C, implying the (cold) tray is initially removing 50 W from the water path!

Given the caveats in the estimates for the total radiated power obtained from the phase 3 data, we now attempt to estimate the radiated power directly. As power is being radiated at different rates both by the outer aluminum skin of TOFr5, and

from the TDIG boards directly through the cover, we need to consider these two processes separately. When 31 °C water is flowing, the aluminum skin temperature is approximately 30 °C, while the TDIG board temperature is ∼38 °C. The radiated power is given by,

$$P_{rad}\ (\text{Watts}) = e\ \sigma\ A\ (T_h^4\ -\ T_c^4), \tag{4}$$

where e and A is the thermal emissivity and the area of the surface, respectively, T_h and T_c are the elevated and room temperatures, respectively, and σ=5.67×10^{-8} W/m^2/K^4. The thermal emissivity [7], e, of commercial sheet aluminum (*i.e.* unpolished and not heavily oxidized) is 0.09, while the thermal emissivity of FR4 (*i.e.* the electronics boards) is ∼0.8. The total surface area of the TOFr5 outer aluminum is 10.8 ft^2, while the total area of the upper surface of the TDIG boards is 4.5 ft^2.

The resulting radiated power estimates are thus 3.3W from the aluminum skin, and 30W from the TDIG boards. As the perforation holes total 50% of the tray cover, approximately 3.3+(30W/2)∼18W would be expected to radiate off TOFr5. This is consistent with the estimate of 20W obtained from the phase 3 data.

Note that this 29.9W estimate of the power radiated by the TDIG boards ignores the components. While these are small in area, they can be significantly hotter. The net result would be an increase in the estimate for the total power radiated by the TDIG boards of a few Watts. This is at a level that is small compared to the measurement errors in this analysis. Improving these estimates would require a more complete treatment of all of the mechanical components in the system, and their interactions via all possible thermal paths, using a full thermal simulation package such as is available commercially.

Nonetheless, the facts that the water loop improves in efficiency in phase 8, and that these power estimates imply that most of the radiative power is coming off the TDIG layer and not the aluminum skin, seem to imply that a perforated cover would not be the optimal approach for the full system in STAR. With a solid cover, the heat radiated by the TDIG layer would be captured on the cover, which has an all-metal thermal path to the flowing water. In this case, one would expect ∼130±10 W would be removed by the water path and the rest, ∼5±10 W, would be radiated into the inside of STAR. The power estimates in kW for the different heat exchange processes and for a full system of these two designs are given in Table IV.

3.5 Cold Water Test

The water available for these tests comes out of the wall at a temperature of 31 °C, which is approximately 7 °C hotter than that available at the tray when TOFr5 is installed in STAR and used so-called 'modified chilled water'. In phase 2, we added ice to the heat exchanger in order to cool the water that was input to TOFr5. The results from this phase are discussed in this section.

Shown in Figure 25 are the on-tray and water temperatures versus the read number (∼4s/read) for this phase. The water input and output temperatures are the two lowest curves, while the on-tray temperatures are the rest shown. For a short

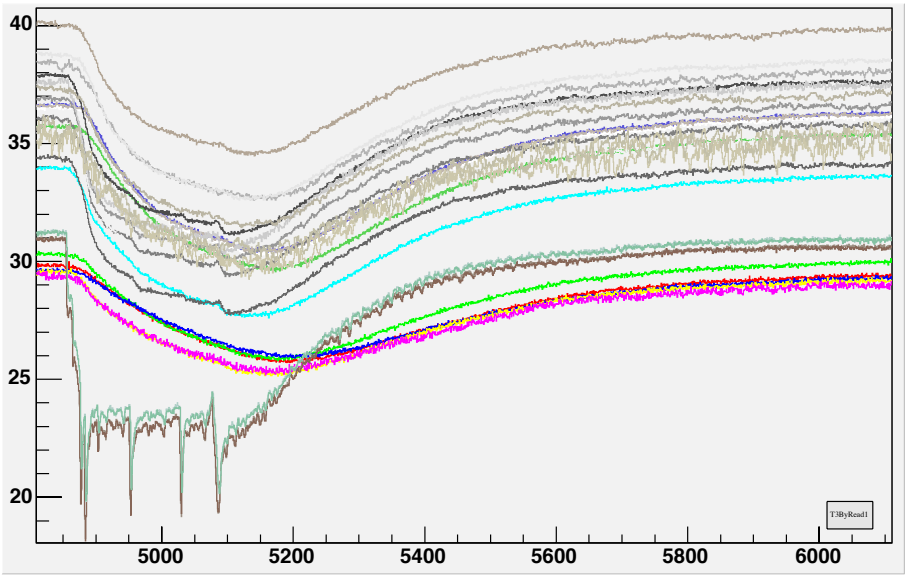


Figure 25: Calibrated temperature versus the read number (∼4s/read) during the cold water test of phase 2.

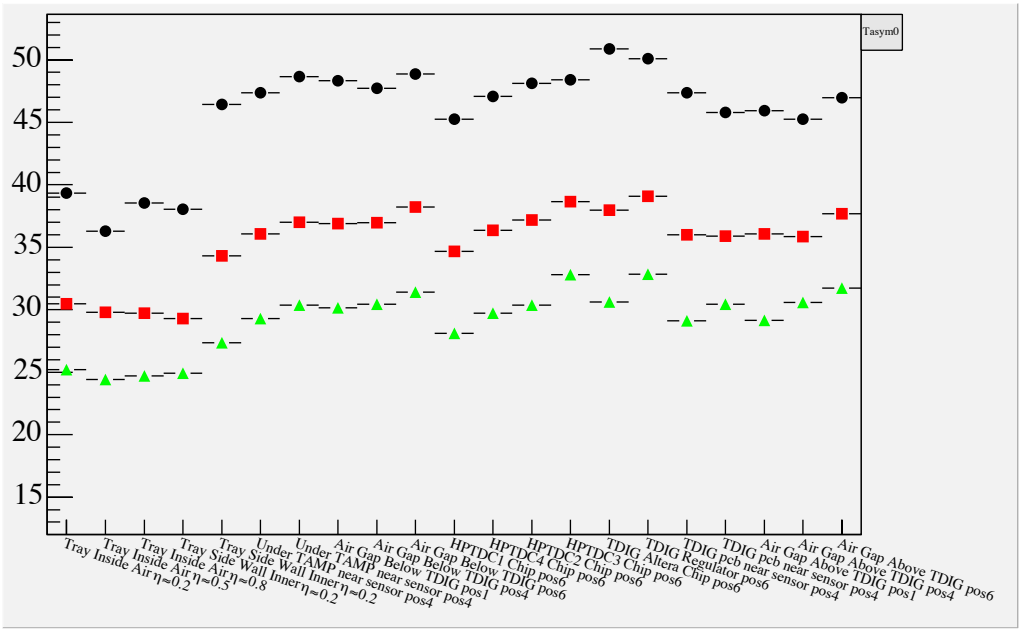


Figure 26: Asymptotic temperatures for phases 0 (black), 1 (red), and 2 (green), extracted by the fits of a constant plus an exponential to the temperature versus time curves for each thermocouple. For phase 2, the fits were performed only over the limited time range where the water temperature at the tray input was near 23 °C.

Design	Power/tray (kW)	Power total (kW)
TOFr5, Water	.105	12.6
TOFr5, Radiative	.035	4.2
TOFr5, Total	.140	16.8
TOFr5 (solid cover), Water	.135	16.2
TOFr5 (solid cover), Radiative	.005	0.6
TOFr5 (solid cover), Total	.140	16.8

Table IV: Estimates for the total power in kW for the TOFr5 design as constructed and for a TOFr5-design but with an unperforated cover, for the different heat removal mechanisms of the water flow and the total radiative processes.

time (∼20 minutes) it was possible to keep the water temperature at the tray input near ∼23 °C. Twenty minutes is not a sufficient amount of time for any on-board temperature to reach an asymptote, as is visible in this figure.

We thus fit the functional form, $par[0]+par[1]*exp(par[2]*t)$, to these temperature versus time curves over the region in time where the water was near ∼23 °C. The values of $par[0]$ extracted from these fits are an estimate for these asymptotes, and are shown versus the on-board thermocouple position as the green triangles in figure 26. The same procedure was also applied to the data from phases 0 and 1 and the asymptotes extracted in this way for these phases are shown as the black circles and the red squares, respectively.

According to this figure, the asymptotic temperatures for ∼23 °C water are approximately 5 °C colder than when the water is at 31 °C. The green points are thus the expectation for the on-board temperatures when TOFr5 is installed in STAR. The asymptotes shown for phases 0 and 1 agree very well with those shown in figure 23, which were obtained by simply averaging the last 2 minutes of temperature values. This indicates that the fitting procedure used to extract the asymptotes for phase 2 is reasonable.

4 Electronics

The requirements for the STAR TOF system outlined in the original May, 2004 proposal specify a system with <100 ps total resolution, σ_t, that is compact and affordable. The STAR TOF electronics design relies heavily on components specifically designed for the LHC project at CERN. The design is based on the CERN HPTDC time digitizer data acquisition chip. The HPTDC has a ∼25 ps LSB and is driven by a 40 MHz external oscillator. It contains more than sufficient buffering capacity to handle STAR data rates. We have demonstrated <25 ps start-minus-stop clock accuracy with the HPTDC in bench tests. The second-generation circuit design TDIG was installed in STAR for the start-side and stop-side detectors for Run 5.

For Run 5, we used Maxim preamplifiers and discriminators to process the MRPC signals, prior to the HPTDC. The total error in σ_t contributed by the electronics is ∼30 ps. This would contribute ∼5% to a 100 ps error in a σ_t measurement.

We have designed a prototype front-end board using the CERN/Bologna-INFN NINO amplifier-discriminator chip. The advantages of the chip would be lower cost, lower power, and perhaps improved timing resolution.

In addition to meeting a timing performance requirement, the TOF electronics must interface to the current and future STAR trigger and DAQ systems, and handle the trigger rates and data rates anticipated at RHIC II. The TOF system will be required to handle Level-0 Accept triggers at 10 kHz and Level-2 Accept triggers at 2 kHz.

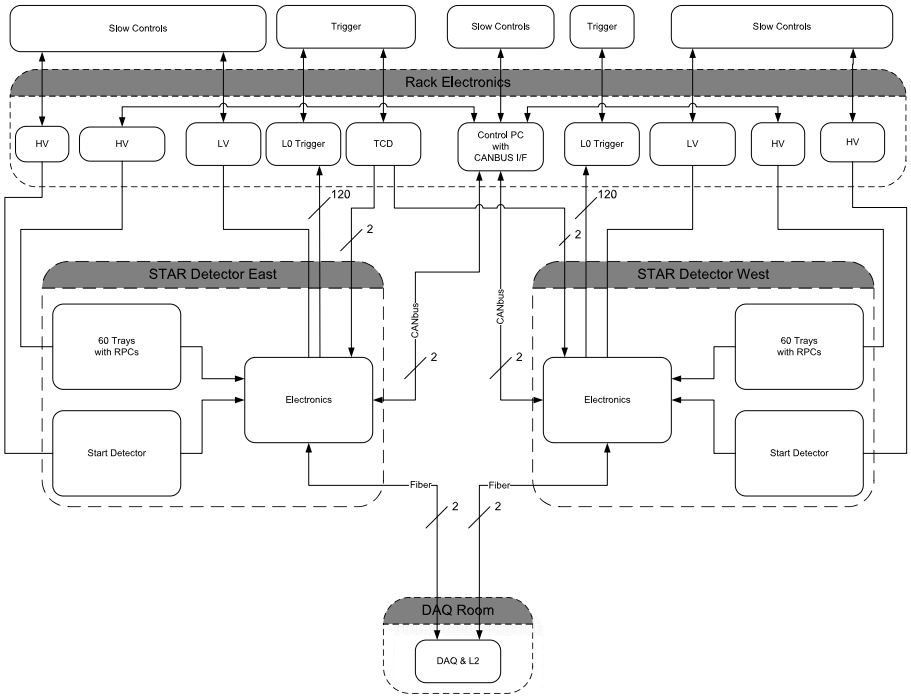


Figure 27: The top-level electronics diagram showing interfaces to trigger, DAQ, and slow controls.

The top-level electronics diagram showing interfaces to trigger, DAQ, and slow controls is shown in Figure 27. The primary detector elements are 24-channel PMT-based start detectors and the 192-channel trays, MRPC-based stop detectors. There are 60 trays and one start detector in each east-west half of STAR or 120 trays and two start detectors in all. All of the electronics for the start detectors are located a few meters from the detectors and all the electronics for the tray are located on the tray.

The electronics are configured and monitored over a CANbus network from a control PC on the south platform, connected by Ethernet to the TOF monitor PC in the STAR control room. There are four interface points to trigger and DAQ. Two are on the west magnet face and two are on the east. There are four dual-fiber connections to DAQ and four, 10- pair copper connections to the trigger TCD from the four interface points. In addition, there are 246 coax connections from the start and stop electronics carrying multiplicity information to Level-0.

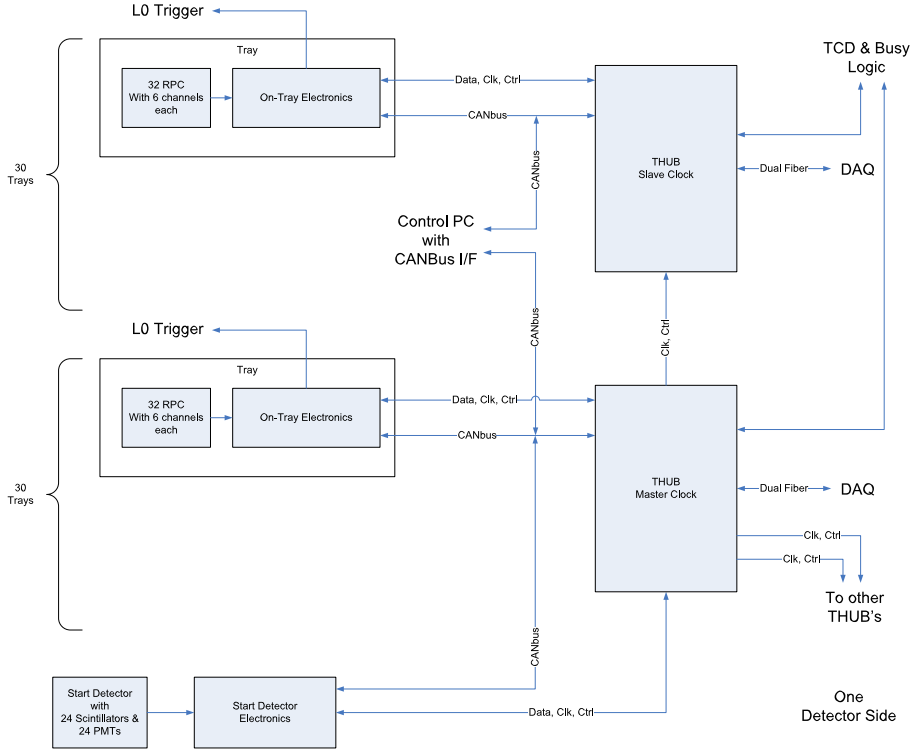


Figure 28: The electronics interconnections in more detail.

The next level diagram, Figure 28, shows the electronics interconnections in more detail. The four interface points to trigger and DAQ are now shown as THUB cards located on the east and west magnet face. Each THUB card (as well as all digital electronics cards on the trays and start detectors) has a 40 MHz oscillator for operation in local or test mode. In normal detector operation, the oscillator on one of the THUB cards is designated as the master clock and provides the 40 MHz external clock for every HPTDC in the system. Each HPTDC has a 21-bit clock counter with a

range of 52 μs. These counters are reset at initialization by a reset command from the master THUB. Due to the different path lengths for the reset signals, each HPTDC counter has a different phase which can be easily learned from the data itself. The fixed phase difference between each piece of data in a TOF event is a powerful tool for maintaining the integrity of the data in an event through many layers of buffering, transmission to DAQ, event building in DAQ, and offline event reconstruction.

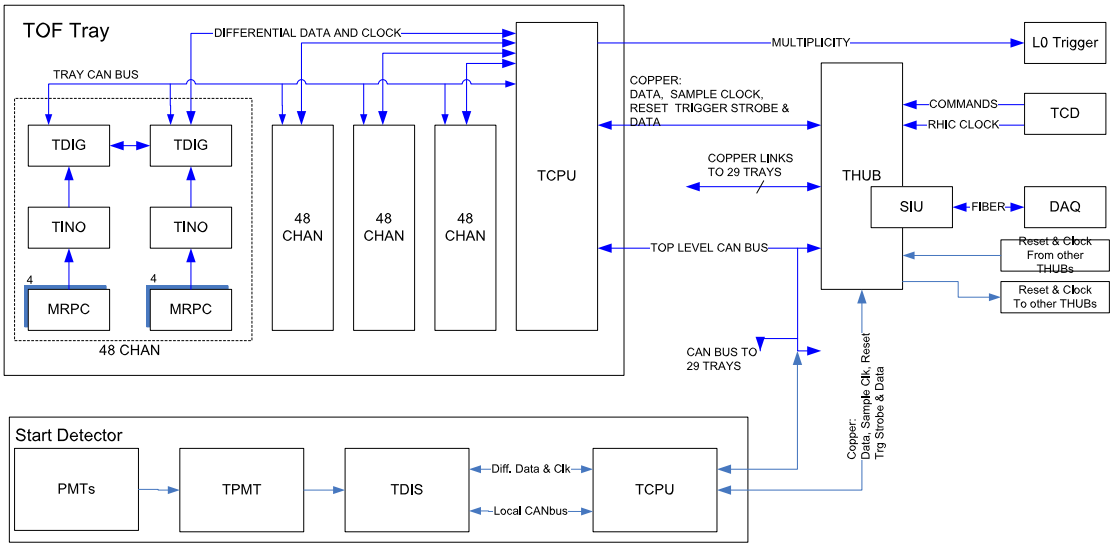


Figure 29: The tray and start detector level electronics.

Figure 29 shows the tray and start detector level electronics. Each tray contains 32, 6- channel MRPC modules. The TINO card provides the electronic interface to the modules. The TINO cards are the gas-tight top of the tray as well. Each tray contains 8 TINO cards and each TINO card serves 4, 6-channel MRPC modules. Each TINO card contains three 8-channel NINO chips which amplify and discriminate the MRPC signals. Each TINO card connects to a TDIG card. Each TDIG card contains three 8-channel HPTDC chips which receive the logical signals from the NINO chip. The HPTDC records a time stamp for the leading edge and trailing edge of each logical signal received and stores them in a buffer. The buffer shared between two channels holds 128 time-stamp pairs. The inter-bunch spacing at RHIC is 0.11 μs and the trigger command is received by the HPTDC $\sim$2 μs following the event so the buffer capacity is more than sufficient.

Each tray contains 8 TINO and 8 TDIG cards and one TCPU card. The TCPU card institutes the readout of the HPTDC on receipt of a Level-0 Accept signal and transmits the data to THUB. As these data are collected and transmitted, the TCPU also builds a bit map of the tray indicating which channels had hits and passes this information to THUB to be passed on to the Level-2 trigger. A similar chain of electronics also services the start detectors except that the TPMT card replaces TINO and only supplies connectivity since amplification of the PMT signals is not required. Besides distributing the clock to each tray and start detector electronics, THUB

provides the only data path from the tray and start detector electronics. THUB uses the ALICE/CERN DDL- SIU daughter card to interface over a dual fiber to a DAQ PC in the STAR DAQ room. The DAQ PC uses the CERN/ALICE D-RORC card in a PCI slot to receive the fibers.

THUB passes configuration and initialization information to the tray and start detector electronics that it receives over CANbus or over the fiber connection. It also receives the trigger commands from the trigger TCD. On receipt of the Level-0 accept command, THUB passes signals to the tray and start detector electronics to initiate the read-out of the HPTDC chips. It buffers the data it receives in reply to the Level-0 command. The Level-2 bitmap is passed along to the Level-2 processor over the fiber connection as soon as it is received. The rest of the event information is held in the buffer until an "abort" command or a "Level 2 accept" command is received. The event data is transmitted to DAQ when the "accept" command is received.

The TOF electronics also provides multiplicity information at the STAR experimental clock rate of 9.4 MHz to the STAR Level-0 trigger. This is similar to the information currently provided by the STAR CTB. From each one-half tray, a sum 0-12 is developed. This is the sum of the logical output of each NINO chip which is "1" if any of the eight NINO channels is above threshold. The NINO logical outputs are passed through a 15-60 ns one-shot to make them all fixed-length and passed to TDIG where they are summed asynchronously. The summed outputs are passed to TCPU asynchronously, summed and sent to the Level 0 trigger. The point of the asynchronous summing is that the STAR experimental clock of 9.4 MHz is not used anywhere in the TOF electronics except in THUB to clock in trigger commands from the TCD. The TOF electronics everywhere uses a 40 MHz clock derived from a single oscillator on one of the THUBs. The asynchronous summing of the Level 0 multiplicity information allows this information to be passed to Level-0 with a fixed processing time so that Level-0 will be able to clock it in properly.

Figures 31-36 show the board-level block diagrams for the individual electronics boards. Earlier versions of TDIG and TCPU were used successfully in the STAR experiment in RHIC Run 5.

4.1 Run-5 Electronics

Almost all of the functionality of the final electronic system was in place and used for Run 5 for the 192-channel "TOFr5" tray and two 3-channel start detectors ("pVPD") installed for that run. Figure 30 shows a schematic of the electronics used in Run 5. The THUB card was not yet designed so the TCPU card served as the mother board for the ALICE SIU fiber interface card. The three SIU's on the three TCPUs in the system were connected over dual fibers to two, two-channel ALICE D-RORC cards installed in PCI slots on a dedicated TOF DAQ pc. The pc was connected by Myrinet to the STAR DAQ event builder. Thus the complete path to DAQ that is planned for the full large-area TOF system was installed and commissioned successfully in Run 5.

The TCPU cards also interfaced to the cable from the STAR trigger TCD in Run

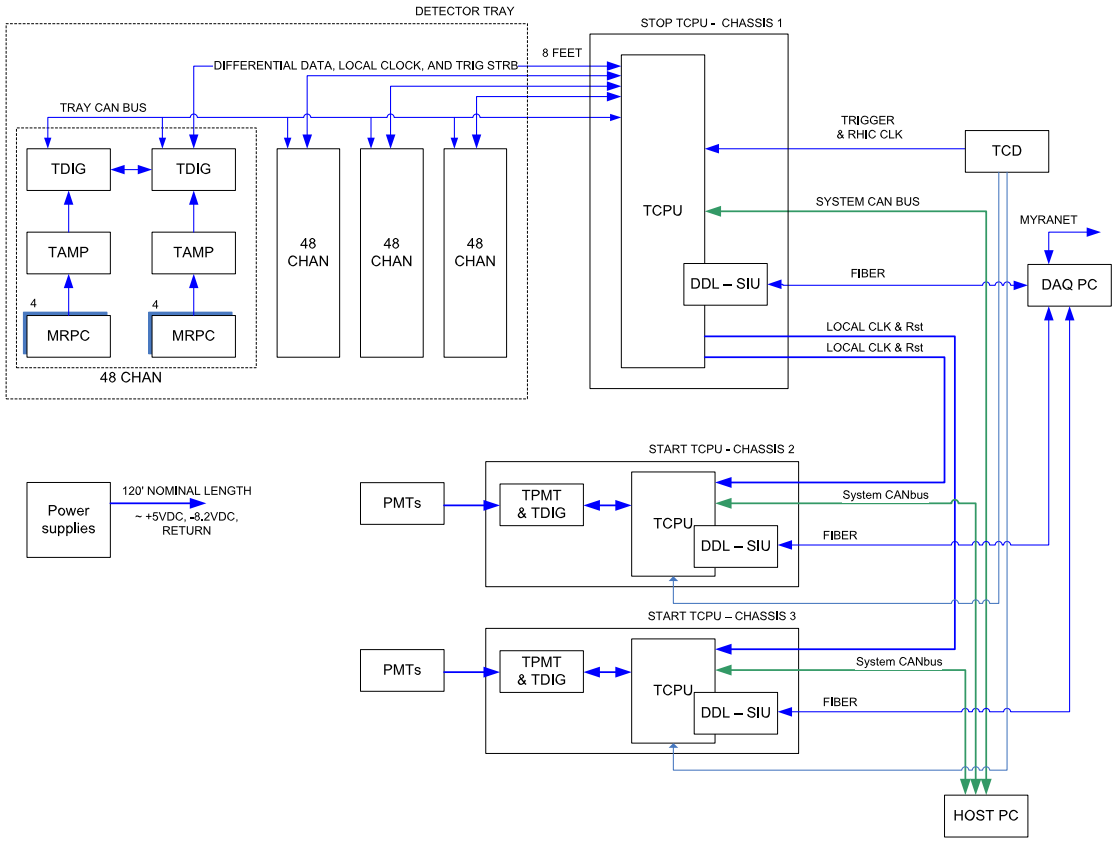


Figure 30: A schematic diagram of the TOF electronics installed for Run-5. Almost all of the functional elements of the final system were in place.

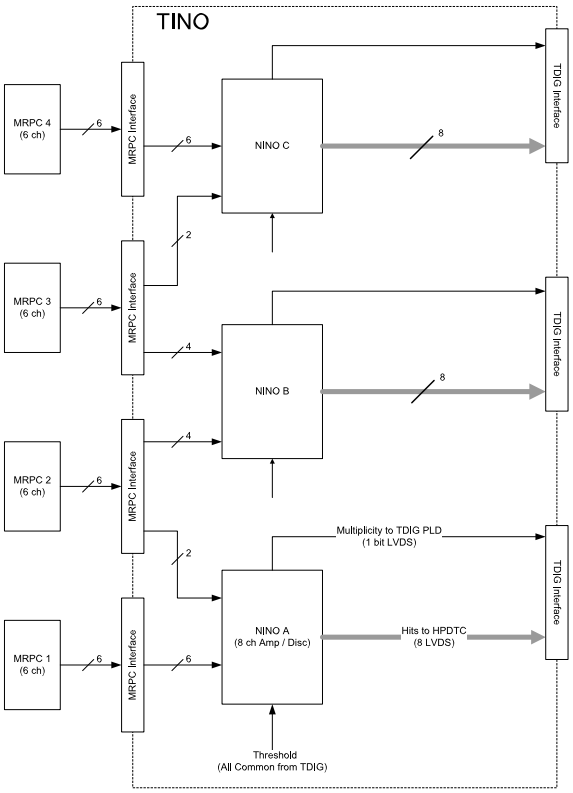


Figure 31: The Front-End Electronics Board "TINO" for amplification and discrimination of the MRPC signals. There are a total of 8 of these boards per tray.

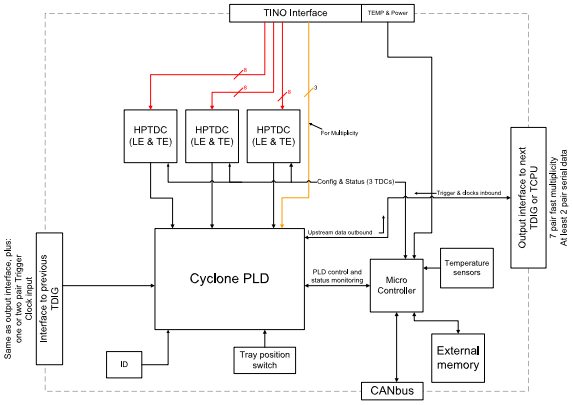


Figure 32: The MRPC digitization board "TDIG". The HPTCD chips on this board digitize both the leading and trailing edge of the MRPC signals coming from TINO. There are a total of 8 of these boards per tray.

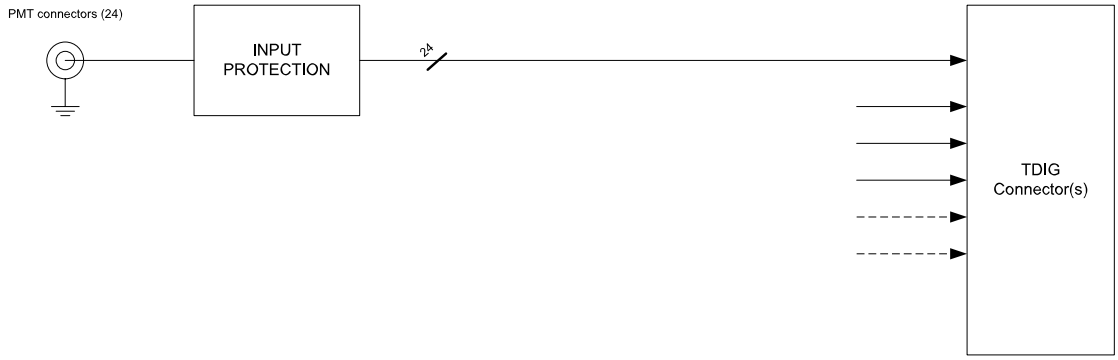


Figure 33: The 24 channel PMT Electronics Interface board "TPMT".

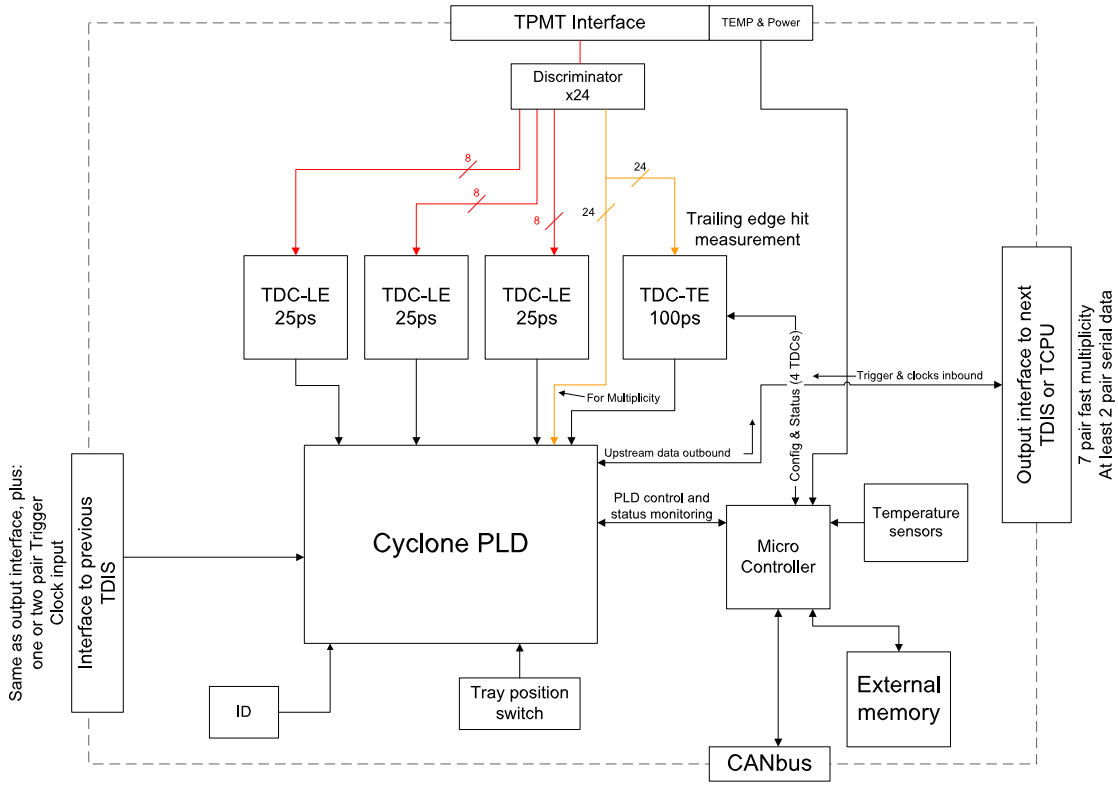


Figure 34: The Start Detector Digitizer board "TDIS". This board is similar to TDIG, but contains one additional HPTDC chip to digitize the trailing edge of the PMT signals from TPMT.

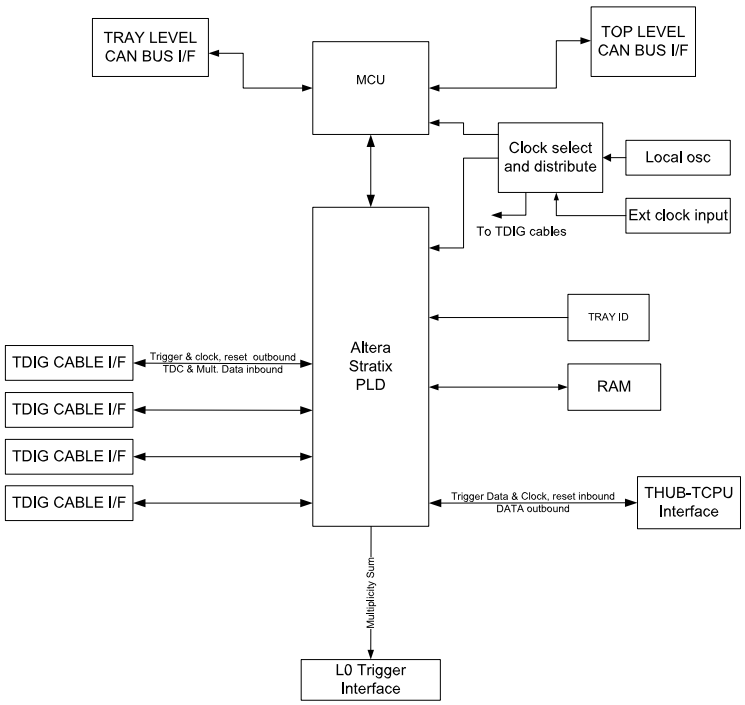


Figure 35: The Data Collector and Controller Board "TCPU".

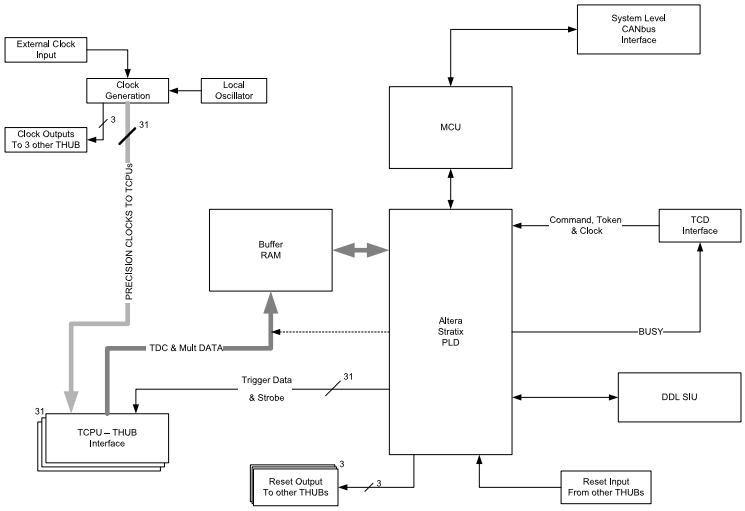


Figure 36: The DAQ and Trigger Interface Board "THUB". Each THUB is capable of interfacing the 31 TCPU (30 trays and 1 Start Detector).

5. This interface will move to THUB in the final system. However, the Run 5 system, once commissioned, successfully interfaced to trigger and DAQ and tens of million of events were recorded for analysis. An analysis of that data is reported in section 7 of this technical update.

Run 5 was also the first use in STAR of onboard digitization and readout using

the CERN HPTDC chip. The TDIG board and HPTDC chip performed well as evidenced by the data taken successfully during Run 5.

The main functional element of the final system that was not tested in STAR in Run 5 is the 9.4 MHz multiplicity input to the Level 0 trigger. This function is included in the initial design of the TINO board and the design of the revised TDIG board that is compatible with TINO. The TINO board will have the same function as the TAMP board used in Run 5 which had component pre-amplifiers but TINO will employ the ALICE/Bologna NINO chip. The chip offers lower cost and lower power and was specifically designed for this function. It also discriminates the input signals so that the comparators on the TDIG board in run 5 can be removed from the revised TDIG board.

Finally, four THUB boards will be added to the system design to remove the need and cost of 122 interface paths to trigger and DAQ that would be required if the Run 5 system were simply multiplied by "120". The new design features required to implement THUB include the interface between the TCPU and THUB cards and an event buffer on THUB that will allow multiple event buffering awaiting the Level 2 Accept command.

4.2 Integral Non-Linearity

The HPTDC chip displays non-linearity in the time bins, which have to be corrected to achieve good timing resolution. These non-linearity are caused by 40 MHz cross talk from the logic part of the chip to the time measurement part and are believed by the chip designers to come from power supply and substrate coupling.

To determine these non-linearity, we use a "code-density test"; a random source of hits (*e.g.* a pulser with a repeat frequency sufficiently different from the 40 MHz TDC clock) is applied to a channel and the resulting distribution of time stamps is plotted. If the TDC time bins were totally linear, the resulting distribution should be flat. Any deviation from a flat distribution is an indication of the amount of "differential" non-linearity.

Figure 37 shows the result of this test plotted for a period of 50 ns (2048 time bins). One can see that the pattern repeats every 25 ns, as the basic TDC architecture is based on a 25 ns unit, using a simple counter to extend the dynamic range. The differential non-linearity for each time bin is obtained from this distribution, and after integrating these non-linearity, one obtains the "Integral Non-Linearity" (INL) distribution shown in Figure 38. To correct time difference measurements for these non-linearity, one uses the 10 LSB of each measurement as an index into a lookup table with the INL corrections.

The left frame of Figure 39 shows a time difference distribution between two hits separated by a fixed cable delay obtained without using the INL correction, while the right frame shows this same time difference distribution after applying the INL correction to each time stamp measured by the HPTDC. In the example shown, the time-difference distribution after the INL corrections shows a resolution of $\sim$20 ps. The INL corrections have a stable shape from channel to channel and from chip to

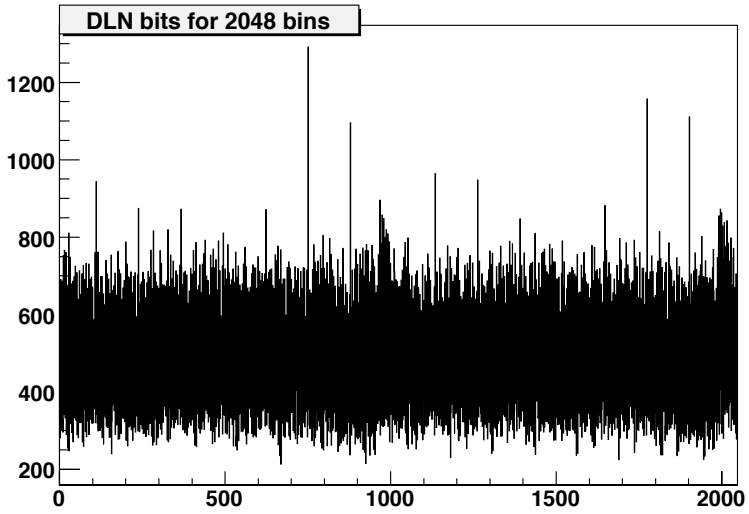


Figure 37: The results of a code density test for a period of 50 ns (2048 time bins).

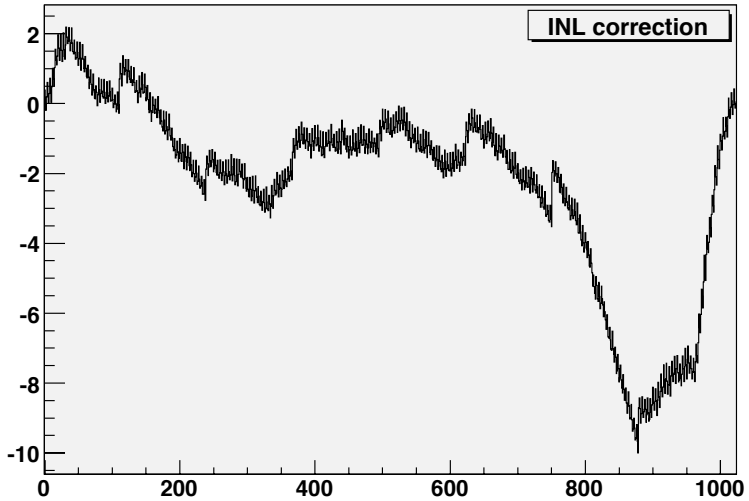


Figure 38: A typical INL distribution. The integrated difference in bins is shown on the ordinate over 1024 bins (25 ns) in the abscissa.

chip. In our tests we have compared using the same INL table for each chip versus a specific INL table for each HPTDC chip, and the results show the same time resolution to within 10%. However, since obtaining a separate INL correction for each chip can be done in parallel, and the INL correction tables are relatively small, we intend to use a specific INL correction for each chip.

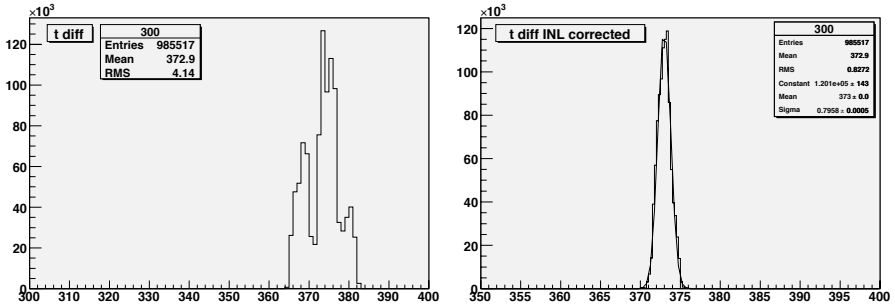


Figure 39: Time difference distributions from a pulser test before (left frame) and after (right frame) the INL correction. The corrected distribution shows a resolution of ∼20 ps.

5 Low Voltage and High Voltage Power Supply systems.

5.1 Low Voltage Power Supply system.

The Low Voltage power supply system (LV) will supply the DC current for TOF front end electronics. Due to the high magnetic fields near the detector and their potential effect on the magnetic materials used in the switching as well as linear power supplies, it was decided to locate these supplies in the electronics racks located on the south electronics platform. In addition to the above requirements, the LV system would require remote control and monitoring. It also needs to be interlocked with the rest of the power systems in STAR.

There are plans to replace the Maxim bipolar discriminators used in the TDIG boards and the pre-amplifier on TAMP with a new chip developed at CERN. These chips, code-named NINO, use only positive supplies, and require much lower power (CMOS circuitry). This would eliminate the tray negative voltage supplies, and also save a considerable amount of power.

In what follows we have assumed that the TINO card using the NINO chip will be used in TOF front end electronics. This choice eliminates the need for negative power supplies and reduces the power dissipation of the trays from 140 watts to less than 100 watts.

In order to minimize conducted and radiated noise, reduce overall power dissipation, and minimize safety concerns, several different power supply configurations have been considered. Of these, three systems best meet the above requirements. These systems are described below in some detail, and are compared to each other in terms of performance and cost. Based on these comparisons, the system that has best cost to performance ratio was selected and used to arrive at the WBS cost estimates.

While systems such as distributed low noise DC-DC converters, *e.g.* VICOR's VI-200 and VI-300 series combined with VI-RAM ripple attenuation modules, have high efficiency, and may be modified to handle high magnetic fields [8], they do

require high input voltages, need additional electronic instrumentation for control and monitoring, and need to be installed and integrated into the tray electronics. Therefore, in terms of cost, and perhaps noise performance, they exceed the costs of the systems considered for the baseline design.

A system which has been successfully used in STAR to supply low noise DC current to the TPC FEEs is the PRM ferro-resonant power supplies from KEPCO. These units are inherently short circuit proof and low noise. A conceptual design using 280 watts off the shelf ferro-resonant supplies (Kepco model PRM 8.5-30) was developed to estimate cost for the WBS. This approach requires some R&D work to modify the existing TPC power supplies and implement new slow controls. Due to bulky nature of these supplies they require more space than low noise switching supplies therefore contributing to overall system cost.

However, the high efficiency (75%) allows one to fit a larger number of these units per rack compared to regulated linear power supply units. As such the overall implementation cost for a ferro-resonant based system would be less than linear regulated power supplies, due to lower cost of infrastructure (i.e. racks and power consumption).

The primary parameter for the design of the LV system is conducted and radiated noise. The importance of this parameter is due to the fact that the MRPC signals are very small, and any external noise coupling to these signals would degrade the timing resolution of the system. The linear power supplies are considered the conventional approach to these type of systems. These units have very low Periodic and Random Distortions (PARD) noise (*i.e.*, 1-2 mV p-p, <0.25 mV r.m.s.) which is mostly concentrated in the low frequency range and could be easily filtered. Unfortunately what they lack is a high efficiency. This contributes to large amount of heat dissipation which would have to be absorbed by external cooling. For WBS cost analysis we considered slightly modified off the shelf linear regulated power supplies [9] with floating output and remote sensing capability. Each power supply unit would supply power to all TINO, TDIG, and TCPU modules installed in a single tray. This scheme isolates trays from each other and eliminates the ground loop problems in the positive supply loop. The actual voltage required at the input to the TOF tray is +4.8 volts.

Figure 40 shows the arrangement of power supply transmission lines per tray and the distribution scheme for the LV power using the regulated linear power supplies. The scheme presented above would require 120 regulated power supplies. Additionally 8 more units would be used for THUB and the start detector low voltage requirements. These supplies would be instrumented with microcontrollers and associated electronics to communicate with an external PC via RS485 (or ethernet) serial bus to control and monitor their functions remotely. Figure 41 shows a possible arrangement of these supplies in a half height rack. As seen in this figure the rack will be instrumented with two chilled water heat exchangers, fan trays, filters and an interlock module which disables the power supplies using the STAR interlock system.

Due to lower efficiency of linear supplies (typically 35%) it is not possible to have a large packing density in the racks. Using the STAR standard rack cooling heat exchanger scheme, i.e. 1200 watts per heat exchanger assembly, one needs a large number of racks to accommodate 120 power supplies. However, due to lack of space in

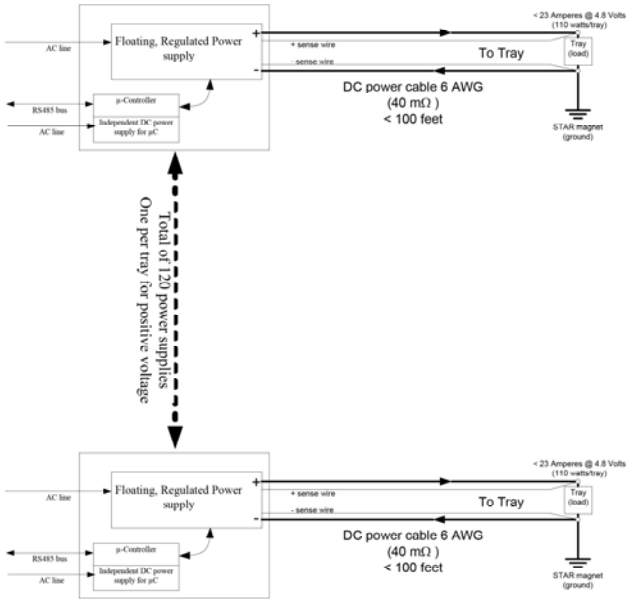


Figure 40: Tray low voltage power distribution scheme.

the south platform one is forced to use the third floor. The wide angle hall clearance requirement dictates that only half height racks could be used on the third floor. As such one is forced to use a total of 18 double bay half height racks to accommodate the entire LV system. The additional cost of supplying the rack space, associated utilities and cooling infrastructure was found to be too high for this option to be a viable alternative.

A third power supply system is Wiener PL-512 (formerly PL500 F8/12) mainframe equipped with MEH power modules [10]. These supplies are ultra low noise switching power supplies equipped with CAN bus and ethernet remote control/monitoring capabilities. Each 3U high supply accommodates 6 MEH modules (each module has two independent floating outputs and could supply up to 210 watts of DC current at a maximum of 7 volts). These are the same type of supplies used to power the STAR EMC FEE crates. The advantage of these units is higher efficiency (85%) and more compact size. A total of 2 single bay full racks would be required to house 12 3U crates of this type which would accommodate the full TOF LV system. Figure 42 shows one arrangement of 6 PL512 supplies with cooling and control hardware installed in a single 40U high STAR rack. This system accommodates 72 independent low voltage channels. Assuming worst case scenario, i.e. bipolar comparator TDIG design (i.e., non-TINO), the total DC output power of a PL512 equipped with 12 channels is estimated at 2400 watts (this assumes 140 watts dissipation in the tray and 54.5 watts in the transmission cables) which using 85% efficiency results in 425 watts of heat dissipation in the rack per PL512 mainframe. For the arrangement of supplies shown in figure 42 the total heat dissipation due to 72 channels is 2.55 kilowatts, while the total cooling power of the heat exchanger assemblies is 3.6 kilowatts. For these estimates we have used 80 feet, 6 AWG conductor pairs for DC power transmission

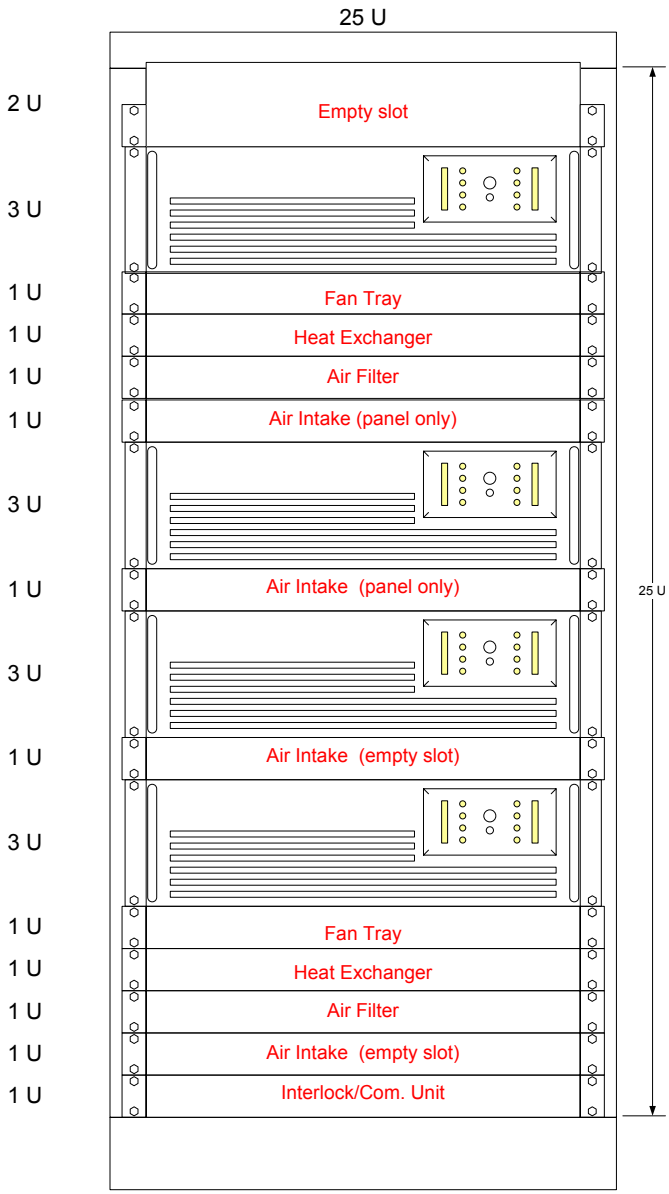


Figure 41: Arrangement of linear power supplies and associated chilled water heat exchangers in the rack for the low voltage power system. One such rack would power 7 TOF trays.

(0.4Ω/1000 feet) which results in 1.87 volts drop in the conductors and 29.17 ampere current per tray at 4.8 volts. The cooling power of heat exchanger assembly is 1200 watts.

Given the higher frequency of the PARD and slightly higher noise levels (i.e., 2.81 mV peak-to-peak compared to 1-2 mV for the linear supplies) it was decided to test the Wiener supplies in the TOFr5 system. A single PL500 mainframe was delivered to TOF group for in situ testing in STAR. This unit was installed and used to power

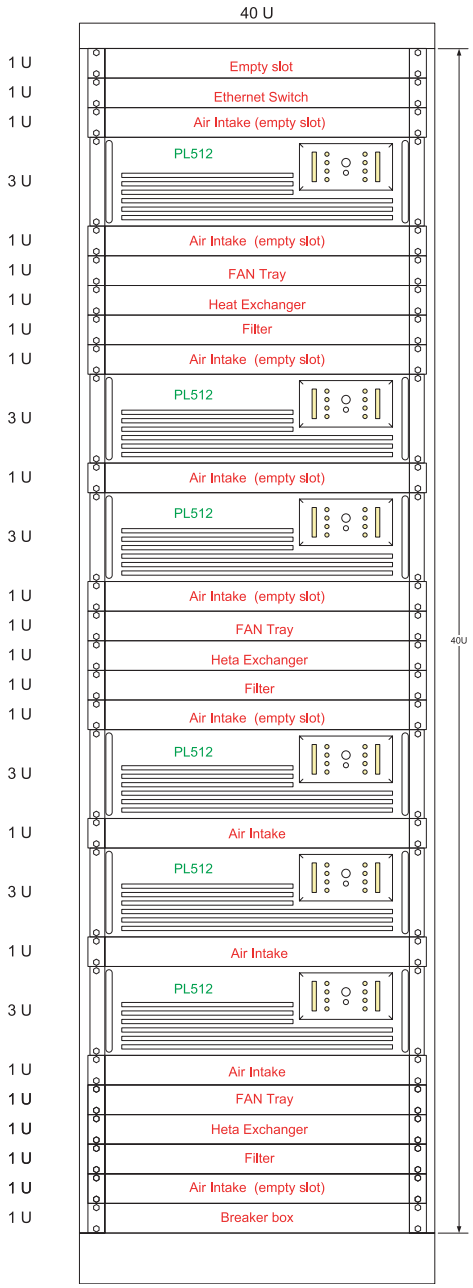


Figure 42: A possible configuration of 6 Wiener PL512 3U high, 12 channel power supplies in a full height rack. This figure also shows the required cooling fans, heat exchangers, air filters, breaker box, and the slow controls interface.

the TOFr5 tray and take data during the period Mar 17 - Mar 31 2005. Figure 43 shows a comparison of the noise rate for the TOFr5 taken with the Wiener PL500 supply (blue solid squares) and the Kepco linear supplies (red solid circles). As seen from this plot the noise rate is virtually unchanged. This indicates that the noise due to the power supply is below the discriminator threshold. Figure 44 shows the results

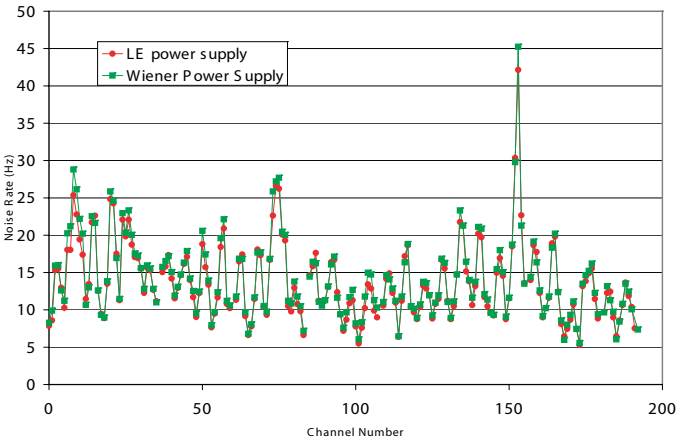


Figure 43: Comparison of noise rates in the TOFr5 tray taken with the Wiener PL500 power supply (solid blue squares) and the Kepco linear power supplies (solid red circles). This data was taken in situ during the March 17-31 data taking period using the slow control CANbus system of the front end electronics.

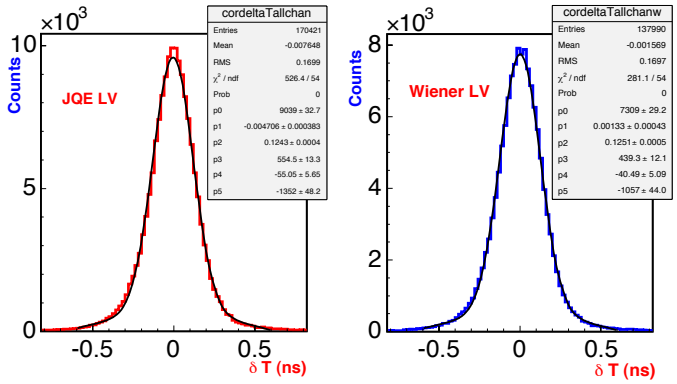


Figure 44: Comparison of the TOF system resolution taken with Kepco linear power supply (left) and Wiener PL500 low noise switching power supply (right). These data were taken during Run-5 62 GeV Cu+Cu running.

of the off line analysis of minimum bias Cu+Cu data taken in the same period. The figures show the timing resolution of the system for all functioning MRPCs extracted with minimum bias events. No statistically significant difference exist between the Kepco linear regulated power supply (left panel) results and the Wiener PL512 low noise switching power supply results (the resolutions are 124 and 125 picoseconds, respectively).

The contribution of the start-time resolution to this result is ∼85 ps due to the low multiplicity in the 62 GeV Cu+Cu minimum bias event sample that was used for this comparison. Figure 45 is another representation of the above result which shows a direct comparison of the TOF resolution extracted from minimum bias Cu-Cu measurements with Kepco linear power supply (red histogram) and the Wiener

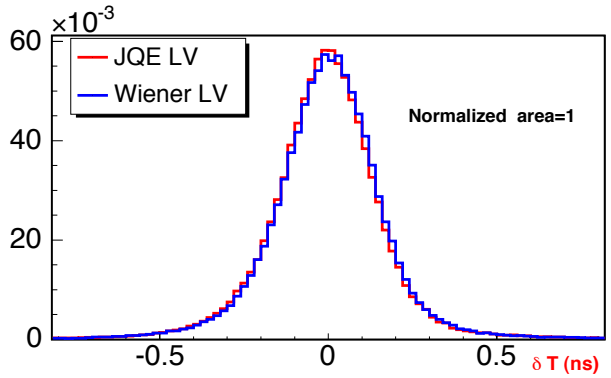


Figure 45: Comparison of the TOF system resolution taken with Kepco linear power supply (red histogram) and Wiener PL500 low noise switching power supply (blue histogram) superimposed on top of each other and normalized to unity. These data were taken during Run-5 62 GeV Cu+Cu running.

PL512 power supply (blue) normalized to unity.

We have decided to use these supplies as our base system to prepare the WBS. We feel confident that the noise levels are low enough that they could be managed by adding additional external common-mode/differential-mode filtering chokes on the cable assemblies. Furthermore due to the length of the DC transmission lines, the higher frequency components of the PARD are expected to attenuate considerably.

One unit has been purchased to be used in the FY2006 run. The results from this run along with planned cosmic ray bench tests should be sufficient to verify the EMI compliance of the LV system with our requirements and whether or not external filtering components would be necessary. It is important to note that due to the lower space requirements, the existing STAR rack space and infrastructure would be able to accommodate the full TOF low voltage system. Additionally, the PL512 cost, which is already the lowest per channel, also includes the cost of slow control hardware, thereby eliminating the cost of hardware development.

As mentioned in the beginning of this section the choice of the LV system was based on the assumption that the TINO card will replace the current comparator-based design. This eliminates the need for negative supplies for the trays, and reduces power consumption from about 140 watts down to 110 watts (maximum). However, all three systems discussed above, namely the Wiener system, the ferro-resonant system, and the regulated linear power supplies do have excess capacity to handle the additional power needs if the original FEE design were to be used. However, additional space (two additional full racks) would be required to accommodate 12 3U fanout boxes to supply negative current to the trays. The 12 Wiener units include one spare which could be used to supply the negative current to all the trays albeit at the cost of coupling the trays through negative supply lines.

In all above designs a slow control system will be developed to remotely control and monitor the LV system. Each power supply unit will have its current, voltage,

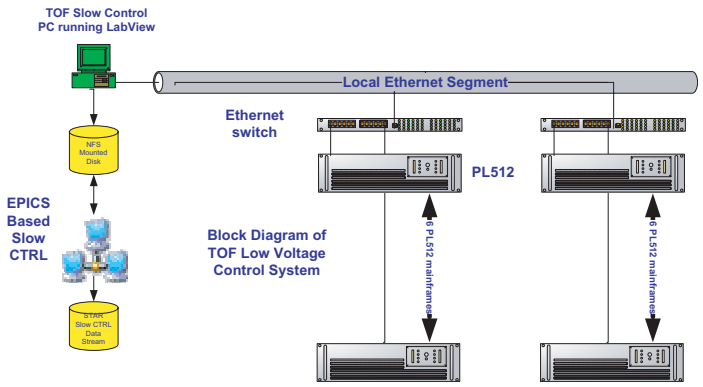


Figure 46: A proposed scheme for slow control and monitoring the LV power supply system using ethernet and TCP/IP to establish communication between slow controls computer and PL512 power supply units.

and temperature monitored independently, and each unit could be turned on or shut down independent of the rest of the system. All units will be interlocked to the STAR main interlock system. Wiener power supplies already have all of the slow control capability built in and will be the easiest to implement. Figure 46 shows a block diagram of a LV control system proposed for slow control and monitoring of PL512 power supplies. In this scheme an ethernet connection using TCP/IP protocol is used to provide communication between the slow control computer and the power supply units. The monitored data is archived on the slow control computer disk which is NFS mounted and could be accessed via STAR EPICS based control system to interface with STAR run controls and alarm system. In addition the data would be available to be sent to the run data stream for off-line analysis.

5.2 High Voltage Power Supply system

The TOF high voltage system will provide ± 7.5 kV to the MRPC detectors. It will consist of at least 1 mainframe equipped with multiple HV pods each supplying ± 7.5 KV to HV breakout boxes. Each breakout box in turn distributes the ± HV to 10 trays.

One such system is depicted in figure 47. The CAEN SY127 mainframe [11] shown in figure 47 is instrumented with three positive (A631P), and three negative (A631N) 4-channel HV pods. Each HV channel could supply 100 μA at 8 KV. The quiescent HV currents of the tray with beam off and with beam on are ∼20 nA and 1 μA, respectively (the beam-on current is the estimated current for the upgraded RHIC luminosity with Au-Au beams). Therefore, a pair of single HV channels could easily supply current to up to 10 trays.

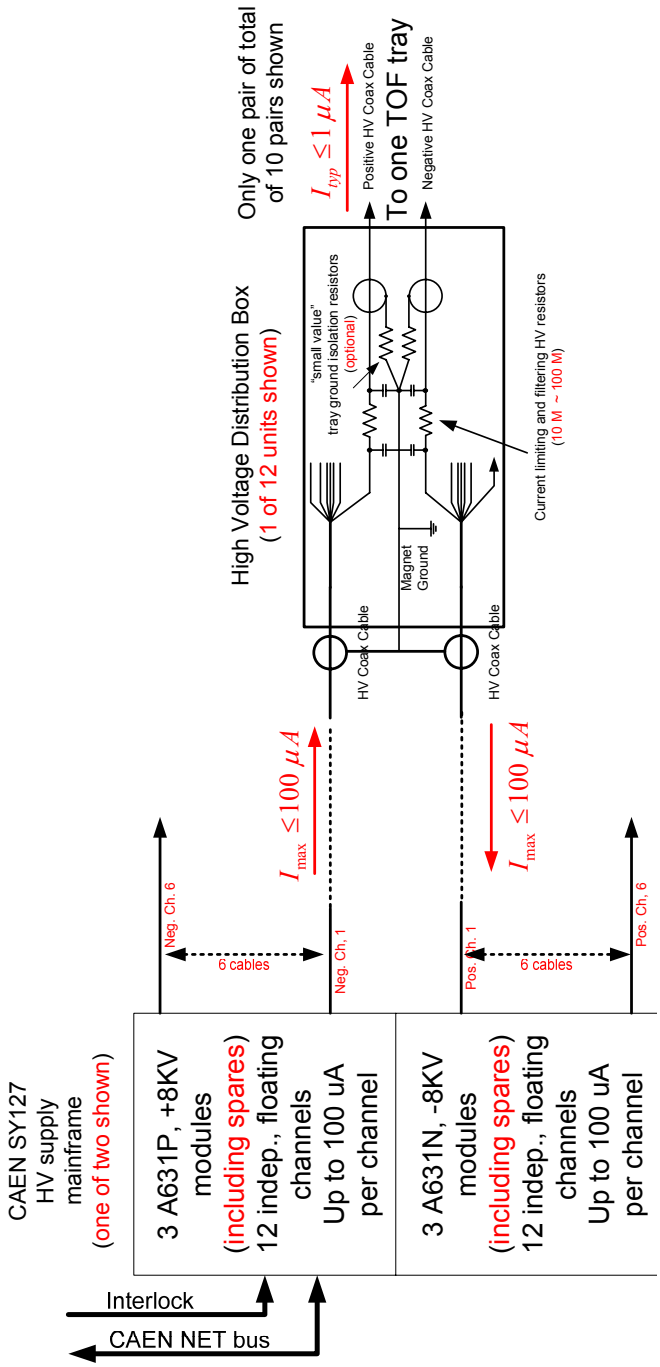


Figure 47: The TOF high voltage distribution system.

The HV shall be controlled and monitored remotely using CAENnet interface installed in a control PC located in the STAR control room. The slow control software shall be developed in LabView. In addition the HV mainframes will be interlocked to the STAR main interlock control system.

6 The Start Detector

The Pseudo Vertex Position Detector (pVPD) [12] was constructed as part of the TOFp[5] Project and has been in operation from Run-2 through Run-5. It is shown in Figure 48 and has provided a wealth of experience on start timing in STAR. This system consists of two mirror-image detector assemblies, one on each side of STAR very close to the beam pipe and at a distance of $|Z|$~5.7 m. Each detector assembly consists of three 2" linear-PMT assemblies fronted by a converter layer of lead and an active layer of scintillator, inside substantial magnetic shields (steel and μ-metal, 3" O.D.). As shielding is used, an equally substantial mechanical structure is needed to withstand the fringe fields from the main STAR magnet.

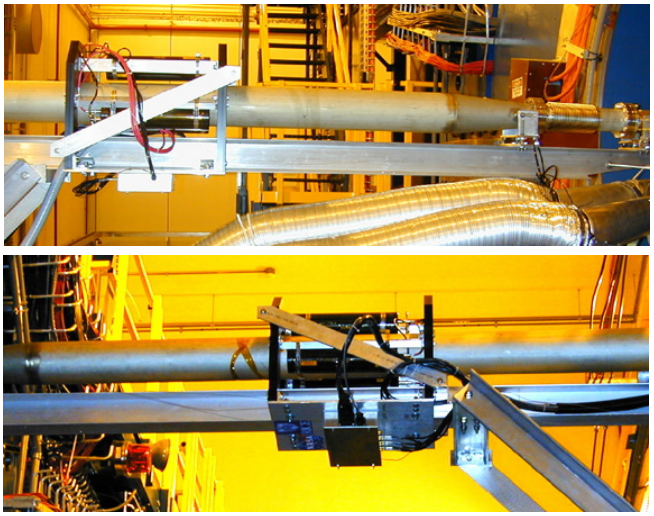


Figure 48: The East (above) and West (below) pVPD during Run-2.

The pVPD was only intended for heavy-ion on heavy-ion collisions, and for these, it has repeatedly shown efficiencies >95% and total start time resolutions as low as 24 ps (in central Au+Au collisions). However, the start timing efficiency of the pVPD in p+p collisions is typically only ~10% per STAR minimum bias event. Unfortunately, it is the case that these p+p events (and p/d+ion and peripheral light-ion+ion events) also result in relatively few primary tracks in the TPC (and TOF) acceptance. Thus, the technique of using solely the stop-side data to infer the start time event-by-event cannot be applied. One needs of order ~6 primary tracks reconstructed to singly-struck TOF cells in order to infer the event start time to ~40 ps (see ref. [13] figure 28 and section 4.3).

The full TOF system would be significantly more efficient for providing the PID of mid-rapidity tracks in minimum bias p+p collisions following an increase in the geometrical acceptance of the start detector. Smaller but still significant increases of the TOF PID efficiency in asymmetric ion and peripheral ion-ion reactions would also

[5]TOFp is the scintillator/PMT-based TOF tray.

result. Such an increase in acceptance can be achieved within the existing integration envelope of the pVPD. By replacing the pVPD's large linear PMTs and their heavy shields with 1"-1.5" mesh dynode PMTs (with much less shielding), a much larger number of PMT detector assemblies can be placed inside the existing integration volume, and yet the overall weight of the system will be similar to that of the pVPD.

Such an upgraded pVPD, referred to here as "upVPD," would also be the required hardware platform to support new (and so far undeveloped) electronics to allow cuts on the primary vertex by STAR Level-0 triggers via fast start-timing. In this sense, the upgraded hardware then supports all of the functionality of the Vertex Position Detector, which has been a part of the STAR conceptual design since the beginning. The TOF proposal [1] provides a general discussion of an upgraded pVPD. The costs for the PMTs and the front-end and digitization electronics for this upgrade are included in the plans and budget for the full TOF system. We discuss the recent R&D on the hardware for this detector in section 6.1. New simulations of the upVPD performance and comparisons to that measured in STAR with the existing pVPD are discussed in section 6.2.

6.1 Start detector hardware R&D

6.1.1 Overview

The technical approach for the upVPD will be very similar to that for the pVPD. Each detector element consists of a Pb converter layer followed by an optically active layer followed by a photomultiplier tube ("flashlight" design). The pVPD uses Bicron BC-420 scintillator as the active layer. Scintillator has the advantage of very high light output, which improves the timing, but also the disadvantages of multiple time-constants in the light production, and a relative lack of radiation hardness. We are also considering Quartz and Lead Glass for the active layer for the upgraded detector as it is more radiation-hard and the light production is prompt, but there is less light overall. The present default is scintillator. In either case the radiator layer is blackened on all sides except that facing the PMT so as to limit the pulse-widening effects from multiple internal reflections inside the radiator.

These detectors are surrounded by an (inner) electrostatic shield which is at the photocathode voltage and an (outer) protective shield of 40mil-thick Aluminum tube which keeps the interior dark. The detector elements are placed inside the existing integration volume of the pVPD.

The 2" linear PMTs of the pVPD will be replaced by 1.5" mesh dynode PMTs for the upVPD. This leads to a number of additional improvements. The detector assembly design is simplified, as the 5 layers of μ-metal plus 2 layers of steel are no longer necessary. The mechanical structure also becomes simpler for several reasons. First, the magnetic forces on the detector assemblies disappear with the replacement of the (magnetic) steel outer shells with (non-magnetic) aluminum outer shells, which allows the mechanical structure to be much less massive. This will decrease secondary production into nearby STAR detectors (PMD and FPD/FMS), an also reduce the

total weight of the system. Second, as the detector elements no longer need a magnetic shield, the mounting of the detectors into the mechanical assembly is also simplified – it will now be possible to simply tap into the outer shell to attach it to the structure.

The pVPD performed well in Run-5 according to preliminary analyses [14]. A prototype of the upVPD will be installed in STAR in advance of Run-6. This prototype will use Hamamatsu R5946 mesh dynode PMTs obtained from the decommissioned TOFp system. The PMTs will be replaced with new ones in advance of Run-8, when major sections of the full TOF system will also be in place.

As the RHIC beam intensities are increasing run-to-run, simple linear resistive bases for the PMTs are not a viable long-term option. Lower-power and higher-rate capabilities will be required. We have already started the development of these bases, as described in detail in section 6.1.2 below. The voltage required is of order -2kV (-2.3kV maximum) and will be provided by the LeCroy 1440 mainframe system that is already in place for the STAR Beam-Beam Counter (BBC). The interface to the STAR slow controls (for control of the individual voltages as well as monitoring) is also already in place and would require only simple changes for the increased channel count.

The digitization of the signals from the start-side will be done using the same electronics as used on the stop-side. This will simplify the offline corrections for the start-side. Also the interfaces to the STAR TRG, DAQ, and slow controls systems will also automatically be in hand as they are the same as on the stop-side.

The start-side digitization is done by the so-called TDIG boards which are the same as those installed on the TOF trays. The only difference in the start and stop electronics is the board just upstream of TDIG - on the stop side it is called TINO, and on the start side it is called TPMT. Both TINO and TPMT exist primarily to feed signals from the detectors to TDIG, and both contain input protection circuits. TPMT is simpler than TINO, however, as the pre-amplification of the MRPC signals needed on the stop-side is not necessary on the start-side.

Such a "modern" electronics path was implemented in STAR in the present Run-5. As the pVPD detectors themselves are extremely well-understood, the data from the pVPD in this run provides an excellent test of the performance of the new TOF digitization electronics. Preliminary timing results are presented in section [14] in this technical update. According to figure 49, the total start-timing resolution of the pVPD in Run-5 is $\sim$57 ps. As the event sample used in this analysis was minimum bias data, and despite the absence of a number of good event cuts that are typically applied, this result is considered good. It indicates that the new on-board digitization electronics are performing close to specification.

6.1.2 New PMT bases for the start detector

In order to improve the high-rate response of the start detectors, we designed and tested two new types of high voltage PMT bases. The main requirements for these bases were high rate capabilities, low power consumption, ability to operate in high magnetic fields, and low cost. The last two requirements eliminated the possibility

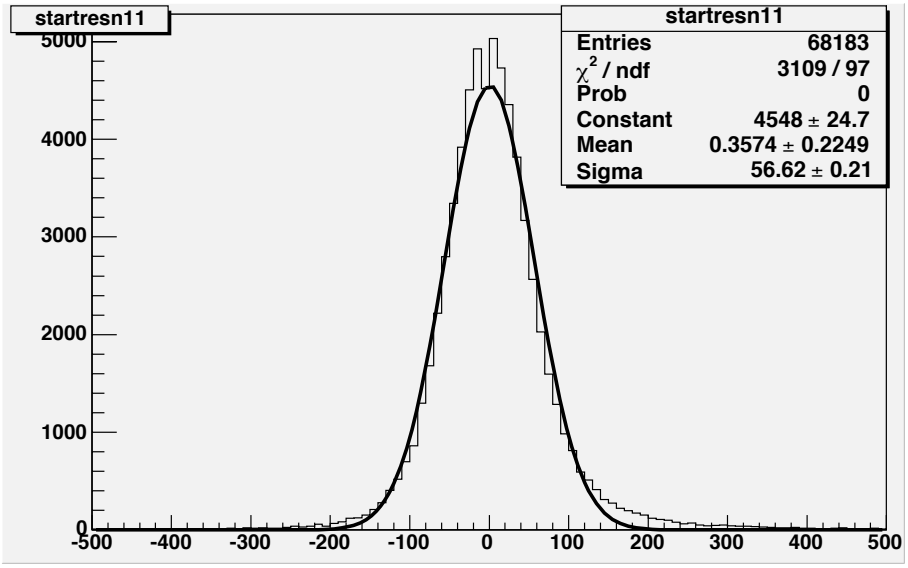


Figure 49: The preliminary total start resolution for *minimum bias* Cu+Cu collisions obtained from the pVPD detectors digitized and read-out using the new TPMT+TDIG+TCPU electronics chain during RHIC Run-5.

of using Cockcroft-Walton style bases *i.e.* a HVSys-style system like that used inside TOFp.

Two different designs were considered for this purpose. The first design was based on the standard Hamamatsu passive voltage divider[6] for the R5946 PMT. In our version, the division ratios were maintained the same as in the Hamamatsu E6113-03 (the suggested default base for the R5946 PMT), while the total resistance was reduced to allow a higher quiescent current. This was done to improve the response at higher rates. The new linear design consumes 2 W of power at -2 kV (1 mA quiescent current). A 1.75" diameter two layer printed circuit board was designed to accommodate the socket and all required voltage divider components. This linear base is shown on the left next to a STAR CTB base on the right in figure 50.

While the new linear design works fine and has, one assumes, the higher reliability of the two designs, it dissipates enough heat that under normal convective cooling the temperature of the bottom of the socket rises to ∼50 °C. This is considered too high since these bases will be potted and enclosed in an aluminum shell in the final configuration. Therefore the component temperatures may be excessive, perhaps causing nonlinearities in the PMT response, damage to the glass envelope of the PMTs, as well as elevated risks of component failure.

In order to address this issue a second class of new high voltage base designs was developed. These "transistor" bases rely on Metal Oxide Semi-conductor FET transistors (MOSFETs) as the primary voltage divider. This approach utilizes the

[6]For example, the Hamamatsu high voltage divider socket assembly part number E6113-03.

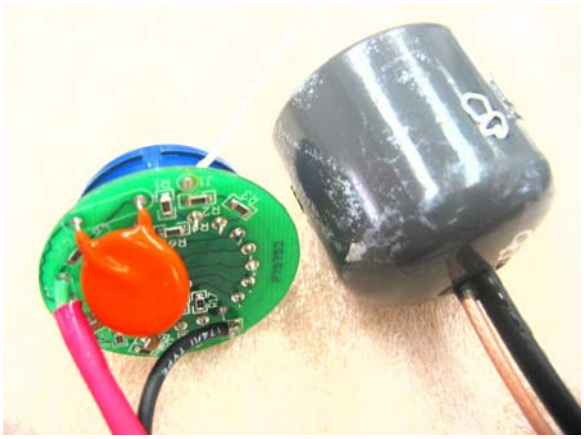


Figure 50: A photograph of the newly-designed linear base (left) and a standard STAR CTB base (right).

very high input impedance of the MOSFET gate to reduce the quiescent current, while maintaining the low impedance of the MOSFET source to supply on-demand high currents typically encountered under higher rates to the anodes. While a resistive divider is used to supply the bias voltages to the MOSFET gates, due to the high impedance of the gate, a much smaller constant (non-rate dependent) current is required.

Three iterations of this design were implemented on printed circuit board designs using surface mount MOSFETs as well as through hole devices. The prototypes from these three iterations are shown in figure 51. In these designs, the current at -2 kV is $1/10^{th}$ of that drawn by the resistive base. Therefore, the power dissipation is also reduced by a factor of 10. The power dissipation could be reduced by an additional factor of 10 by the selection of even higher value resistors without much change in the response of the base. This will be studied in detail in future tests. There are no magnetic field effects on the operation of these bases.

The initial design, seen on the left in figure 51, used a single large square PCB parallel to the axis of the PMT. The two later versions seen on the right reduce the overall size of the circuit. The second version uses two parallel round PCBs. The latest design uses a single 4-layer, double sided PC board with 1.6" diameter, which accommodates all components and the PMT socket. Two of these version-3 transistor bases have been fabricated and tested. A total of four of these bases will be soon be available for use in tests in STAR.

Each base was "burned in" for one week at -2 kV, and its voltage division ratios measured before and after the burn-in period. No changes were seen in these ratios. Also the temperatures were measured on these bases. No discernible differences between room temperature and the bases could be measured. All fabricated units were coated with high voltage conformal coating to eliminate discharges at higher humidity environments, and to protect the components and improve their reliability.

It is important to test these MOSFET based HV divider bases in the actual

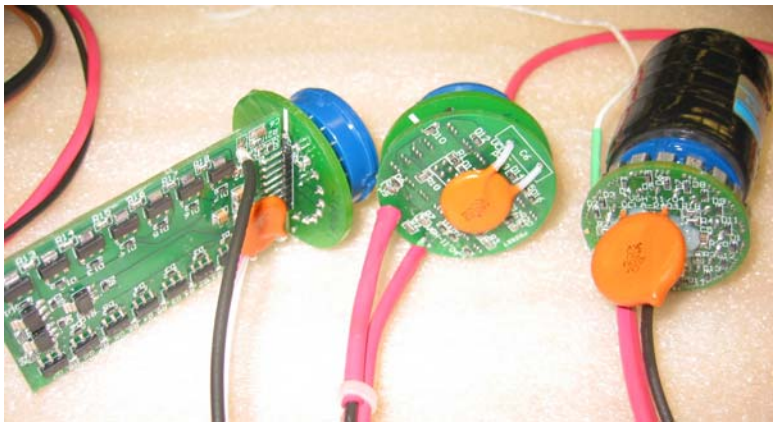


Figure 51: A photograph of the newly-designed transistor bases. The first version is on the left and the third version is on the right. A Hamamatsu R5946 PMT is attached to the latest version for scale.

radiation environment of the start detector to verify the reliability/longevity of these MOSFETs. The MOSFET based voltage divider may be modified to accommodate any voltage division ratio and therefore any other model of PMT. This would require only a new PC board layout. Such a change of PMTs for the start detector from the present R5946 default could occur, as the R5946 is no longer being produced by Hamamatsu.

6.2 Forward simulations

A simulation study concentrating on the very forward areas of STAR near the beam pipe was performed. The main goals of this effort were the following:

- a strict comparison of the forward geometry in star (beam pipe, and pVPD [12]) as defined via "`*.g`" files in the STAR simulations framework to CADD drawings obtained from STAR STSG [15, 16], and any revisions to the existing star geometry needed to make the two geometry definitions consistent.
- the definition in the simulations framework of a number of inactive metal pieces near the beam line that were previously missing from the simulations geometry definitions. The proper inclusion of these pieces could increase the backgrounds seen in any pVPD, PMD, or FPD simulation.
- the definition of new simulations geometry configurations which replace the pVPD of Runs 2-5 with a new, larger-area detector (here called the upVPD), which is needed to improve the start time efficiency in p+p and light-ion reactions for the large-area STAR TOF system [1].
- the GEANT simulation of minimum bias p+p and Au+Au events through these updated or new geometries to compare the performance of the different designs for the upVPD.

The various detector geometry options are controlled via the `geometry.g` file after the user-specification of the configuration name. The configuration names studied here are the following.

- **Y2004X** - This is the current library version of the STAR "standard" geometry configuration. This is unchanged in the local code with the following exceptions. First, a bug was found in the orientation of the "boats" for two of the three pVPD PMT assemblies one each side, which was fixed. Second, the pVPD FEE box is mounted onto a side-strut of the pVPD in Runs 4 and 5, whereas the Y2004X pVPD geometry places it under the pVPD base plate (as it actually was in Runs 2 and 3). This was fixed. Third, the thickness of this (Aluminum) electronics box was incorrect - it was 0.25" but should be 50 mils. Other than these trivial modifications, Y2004X should be considered as a close reflection of the forward geometry presently used throughout STAR. Note also that in this "standard" geometry, the only component to the pipe support structure that is defined in the simulations is the 4" I-beam itself.

- **Y2004Y** - This version makes additional changes to the Y2004X configuration in two major areas. The first of these is the new definition of the components of the pipe support structure. These components include the "cross-piece" underneath the I-beam, the diagonal struts of 3" aluminum angle that support the cross-piece from the balcony, the vertical pieces of aluminum angle at the highest-$|Z|$ extent of the I-beam, as well as the brackets and bolts that hold the pipe in place with respect to the I-beam that are near the lowest-$|Z|$ extent of the I-beam. Also defined is the long threaded rod that holds the pipe support structure in place laterally with respect to the pole tip. This rod does not exist in the latest STSG CADD so a position and diameter (3/8") for this rod was invented based on photographs. The second group of changes involved modifications to the positioning of all of the forward hardware with respect to Z-position of the magnet steel to match the (updated) CADD files. To make the simulated hardware match up with the CADD and the photographs, it was necessary to change geometry parameters for the I-beam, the pVPD (both in `vpddgeo.g`), and the beam pipe (in `pipegeo.g`). Also implemented for the first time in this configuration (and the later ones below) is the 3/4" offset between the East and West balconies with respect to STAR that I discovered about a year ago. This offset was recently confirmed [16] and subsequently included into the STSG's CADD files.

- **Y2005** - This version is the same as Y2004Y, except for a single change. The pVPD Z-positions were changed to match STAR as it exists right now during Run-5. In the previous runs, the pVPD was positioned symmetrically with respect to the I-beam support structure, specifically the "cross-piece."[7] For

[7] Hence the 3/4" East/West balcony offset is visible in the pVPD Z-positions defined in `vpddgeo.g` based on the configuration name.

Run-5, STSG positioned the pVPD equidistantly East and West from a piece on the BBC [17], and the pVPD Z-positions used in this configuration are those that were directly measured with respect to the BBC following the pVPD installation for Run-5.

- **Y2006A** - This version is the same as Y2004Y or Y2005, except that the pVPD, with three 2" PMTs inside 3" O.D. steel shields, is replaced by detector with more channels in the same integration volume. Assumed for this detector are 1.5" PMTs (*e.g.* the Hamamatsu R5946 mesh-dynode PMTs used in TOFp and the CTB) inside 2" O.D. thin-walled Aluminum cylinders. In the Y2006A configuration, nineteen (19) such detector assemblies are placed in a non-cylindrically symmetric arrangement due to the presence of the pipe support I-Beam just under the pipe.

- **Y2006B** - This version assumes the same 2" OD detector assemblies but places twenty-two (22) of them cylindrically-symmetrically around the pipe in two rings. This was achieved by lowering the I-beam with respect to the pipe by 2.25". The present pipe support brackets seem capable of allowing such a shift without modification.[8]

- **Y2006C** - This version assumes the same 2" OD detector assemblies but places thirty-three (33) of them cylindrically-symmetrically around the pipe in three rings. This was achieved by lowering the I-beam with respect to the pipe by 3.25". The present pipe support brackets seem capable of allowing such a shift with the only modification being the replacement of the present vertical bolts with longer ones. Note that the detector assemblies in all designs above have long axes parallel with the beam axis, while the third ring in the Y2006C geometry is at a radius $R\sim$17cm. A Y2006D geometry was built and tested for which the upVPD Pb layers were placed in the same (R,Z)-positions but the positioning of these detector assemblies included a phi-dependent angle to "point" the detectors at Z=0. The Y2006D results were indistinguishable from the Y2006C results.[9]

Multiple views of these six modified or new configurations are shown in Figure 52 - the views of Y2004X are in the upper left frame, while the views from Y2006C are seen in the lower right frame. In each frame, a side view of the entire beam pipe and support structure is shown at the top. Just below this is a close-up of this hardware on one side (the East). Just below this and to the right is a side view of a detector assembly. At the bottom left is an isometric hidden-line view, and on the bottom right is the view along the pipe.

[8] Such a shift could cause an interference with the PMD. If this turns out to be the case, one could imagine simple revisions to the I-beam itself to clear such a conflict.

[9] The outer ring of detectors in Y2006C only needs to be rotated radially by 1.7 degrees to point to Z=0, hence all start detector assemblies can simply be parallel to the Z-axis for mechanical simplicity without significant loss of geometrical acceptance.

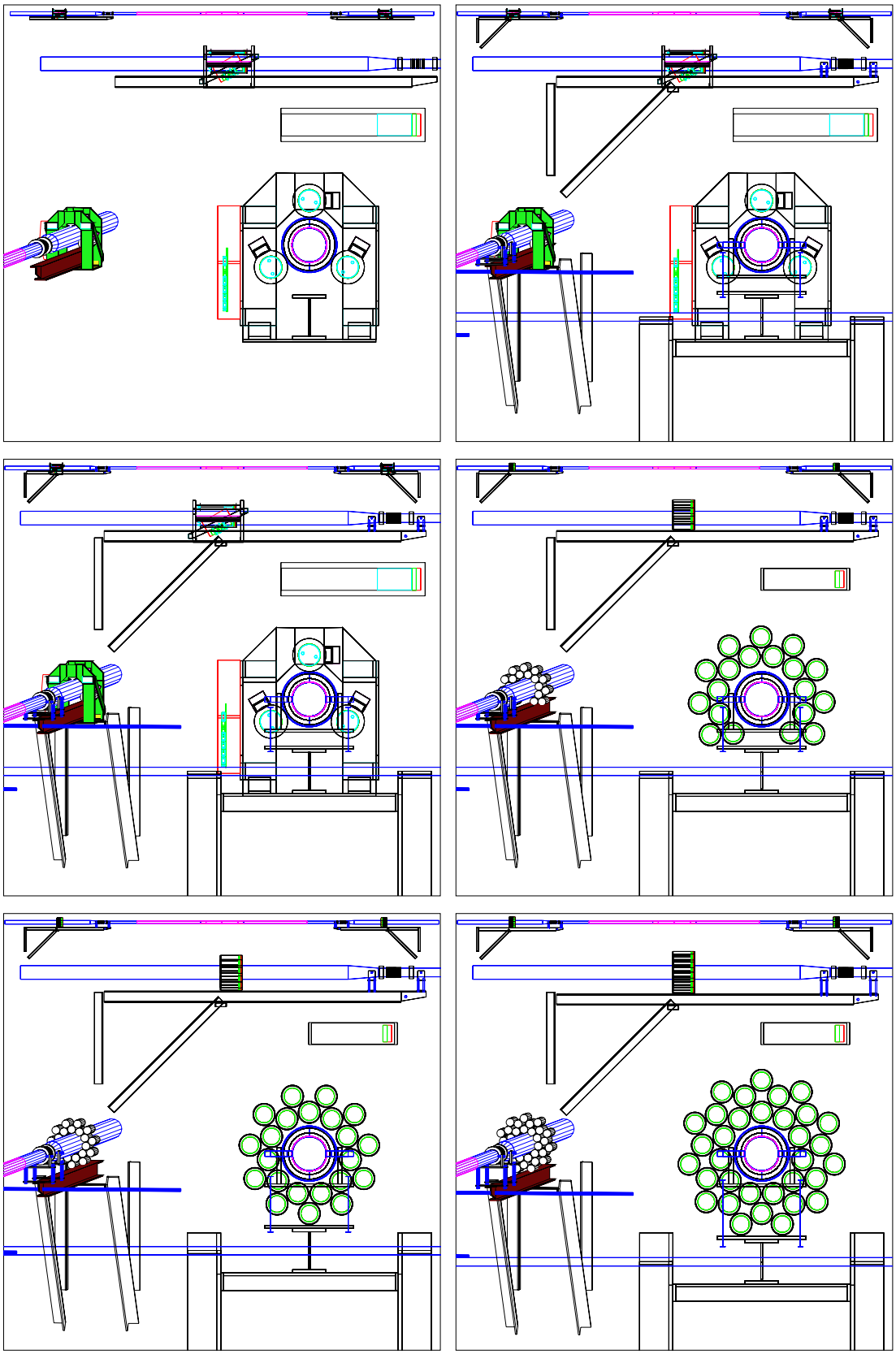


Figure 52: Geant renderings of various views of the new simulations geometries; from upper left to lower right: Y2003, Y2004X, Y2004Y, Y2005, Y2006A, Y2006B, Y2006C.

The comparison of the upper two frames of Figure 52 indicates that both the beam pipe's "transition region" and the pipe support I-beam have been moved outwards in $|Z|$ in the present versions of the simulations geometry in order to match the STSG's CADD files. The new materials added to the forward geometry (I-beam support pieces, pipe support brackets, *etc.*) can be seen by comparing Y2004X (upper left) with any of the other views.

The three "2006" geometries replace the pVPD with the upVPD which has more, but lower diameter and much lower mass, detector channels. Such an increase in the number of channels in the start detector is needed to increase the start detector's efficiency for providing start times to the full TOF system in low-multiplicity events such as those from p+p, asymmetric ion, or peripheral heavy-ion, collisions.

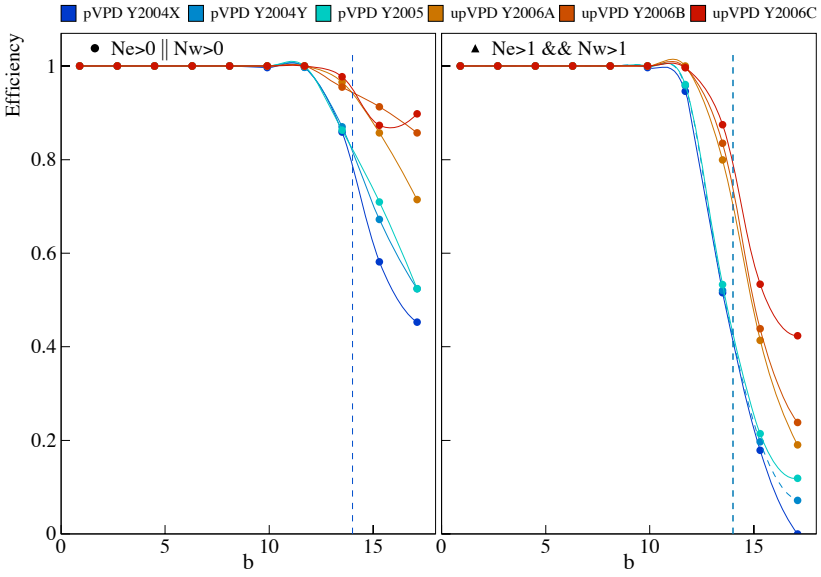


Figure 53: The efficiency per event of the various designs of the (u)pVPD versus the impact parameter in femtometers from the full simulation of minimum bias Au+Au events from HIJING. The vertical line at 14fm is twice the hard-sphere radius for Au.

Shown in Figure 53 are the start detector efficiencies per event versus the impact parameter, b, in minimum bias Au+Au collisions for the different (u)pVPD geometries as labelled across the top of the figure. The three cooler colors depict the pVPD in the (incorrect) STAR default Run-4 geometry, the corrected Run-4 geometry, and the corrected Run-5 geometry, respectively. The three warmer colors depict the results from the various versions of the upVPD. In the left frame is the start detector efficiency per event using the condition that there was at least one hit on *either* the East or West sides, and on the right is the efficiency per event using the condition that there was at least one hit on *both* the East or West sides. As has been seen experimentally in Runs 2 and 4, the pVPD efficiency is excellent in Au+Au collisions, and only tails off for extremely peripheral impact parameters. The various upVPD

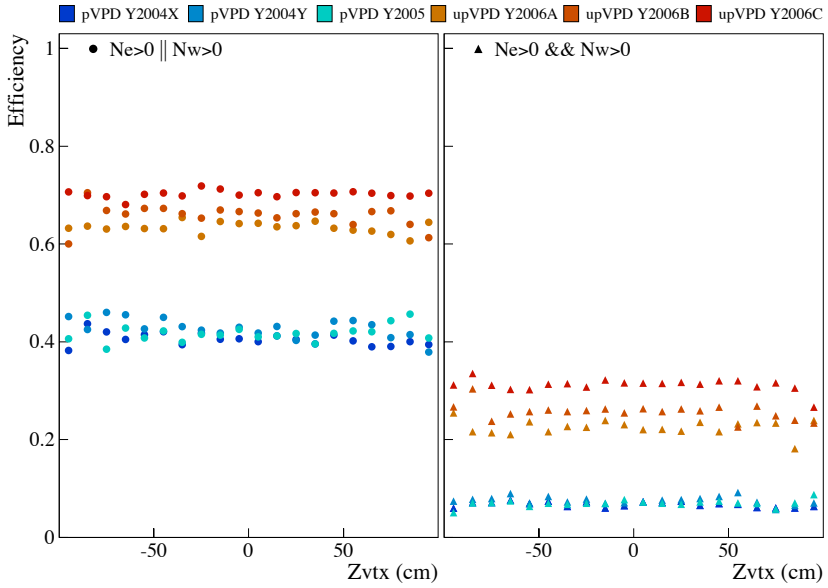


Figure 54: The efficiency per event of the various designs of the (u)pVPD versus the Z-value of the primary vertex from the full simulation of p+p events from PYTHIA. The efficiency for at least one hit (east or west) is shown in the left frame, while the efficiency for at least one hit on both the east and west is shown in the right frame.

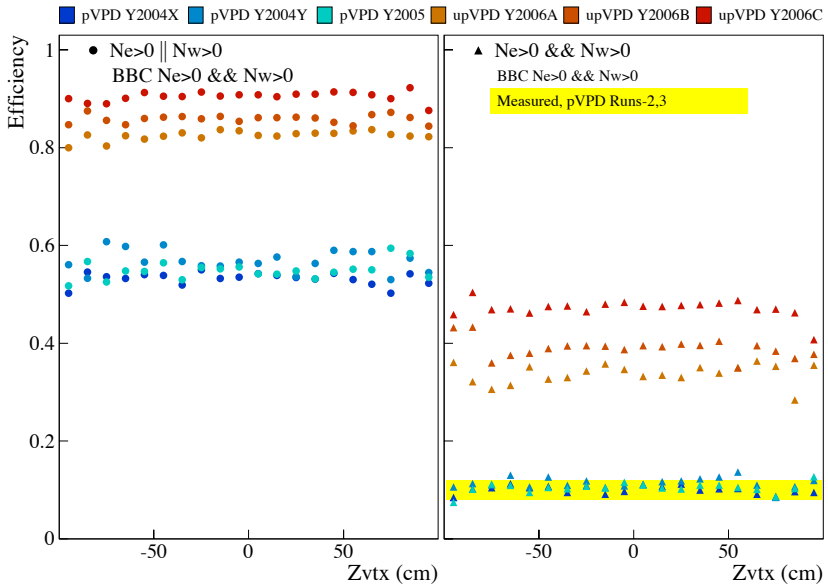


Figure 55: The same as figure 54 but including the requirement that there was at least one hit in both the East and West BBC detectors in the same event. The yellow band depicts the values observed experimentally during the p+p phases of RHIC Runs 2 and 3.

designs are of course also perfectly efficient for $b \lesssim 11$fm, and have a slightly improved efficiency for the most peripheral collisions.

Shown in Figure 54 is the efficiency per event of the various designs of the (u)pVPD versus the Z-value of the primary vertex from the simulated p+p events. The two frames correspond to the same two "local trigger" conditions as used in figure 53. No significant Z_{vtx} dependence in these efficiencies is observed. The efficiencies per p+p event increase significantly when comparing the pVPD geometries to the upVPD geometries, due to the larger number of detector channels in the upVPD. The Y2006C upVPD geometry with 33 detectors in a cylindrically-symmetric arrangement has a 10-15% better efficiency per event than the Y2006A upVPD geometry of 19 detectors in a non-cylindrically-symmetric arrangement.

Shown in Figure 55 are the same efficiencies as shown in figure 54. In this figure, however, only p+p events that result in at least one hit in each of the East and West halves of the BBC are included. This sample of events is expected to more closely match those that STAR collects during RHIC p+p running, since such a condition on the BBC is typically required at Level-0 during data-taking. For these pseudo-"STAR-triggered" events, the (u)pVPD efficiencies are significantly higher than those for the true minimum bias p+p collisions used to make figure 54. The upVPD efficiencies for the "$\geq$1.or.$\geq$1" local trigger (left frame) exceed 80% for all three upVPD designs. It is $\sim$90% for the Y2006C design. The efficiencies for the "$\geq$1.and.$\geq$1" local trigger (right frame) exceed $\sim$35% for all three upVPD designs. It is $\sim$45% for the Y2006C design.

The yellow band indicates the local trigger efficiencies observed from the actual pVPD in the p+p phases of Runs 2 and 3. The experimental values are in the range of 8-12% per STAR event, which presumably would have been triggered via the CTB in Run-2 and both the CTB & BBC in Run-3. The present simulations for the pVPD configurations (bluish points in the right frame) are consistent with this observation once the BBC requirement is included in the simulations to simulate the Level-0 trigger.

6.3 Prototype for Run-6

A prototype "large-area" start detector will be installed in STAR for Run-6. This detector will have 19 PMTs on each side, and be read out using the same electronics that were used in Run-5.

The mechanical design of this Run-6 prototype is shown in Figure 56. The three views across the top of this figure indicate the installation procedure. On the left, only the mounting brackets are installed onto the beam pipe support I-beam. In the center, one-half of the clam-shell mechanical structure is installed onto the brackets. On the right, both clam-shells are installed. Unlike the pVPD, the clam-shell mechanical structure of this prototype does not require additional adjustments to the detector positioning once the mechanical structure of the detector is installed. This significantly reduces the time needed to install (or remove) these detectors compared to the existing start detector.

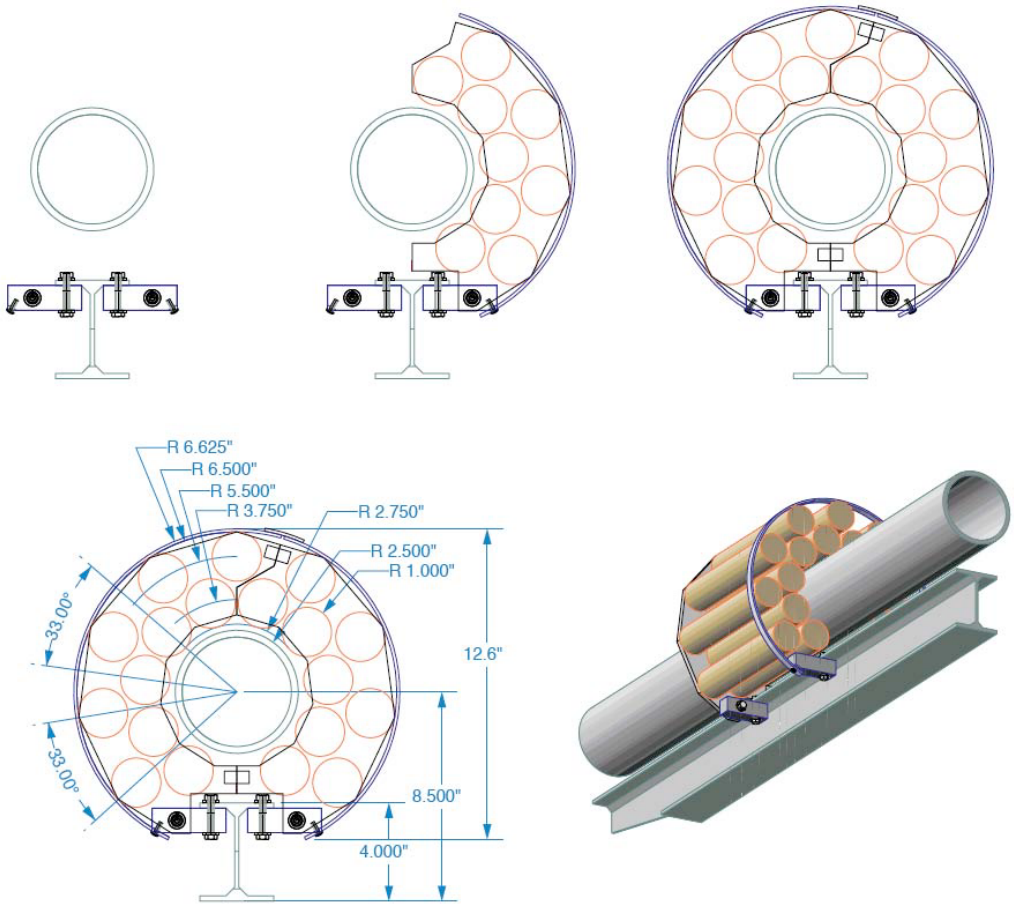


Figure 56: Various views of the Run-6 Prototype of the "large-area" start detector upgrade.

The PMTs are the Hamamatsu R5946 PMTs that were once in the TOFp tray. All of the PMTs have been removed from their TOFp slats, and have been tested for dark current and gain using a radioactive source and a small test scintillator.

7 Preliminary Analysis of the Run-5 Data

RHIC Run-5 marks the first attempt at a number of important steps towards the full system. Most importantly, the NIM/CAMAC-based local trigger and DAQ systems provided by the TOFp system are replaced by new electronics (TAMP/TDIG/TCPU) that do the digitization on-board with respect to a 40 MHz clock. The data path to STAR DAQ over optical fiber also includes new electronics developed for the LHC. These are the first attempts at using these electronics in a running experiment.

In this section, a preliminary analysis of the Run-5 data from TOFr5 in STAR is described. This analysis was performed in two parts. The first part is an analysis of the start-side information from the pVPD, which allowed the first timing resolution estimates of the new electronics. This first analysis thus uses the TOF raw data. Several months later, the STAR tracking information became available. The second part of this analysis thus used the so-called STAR "microDSTs" and concentrated on both the start and stop sides, the total resolution of the system, and the PID performance. The discussion below is as abbreviated version of the more detailed write-up available in Ref. [20].

7.1 Analysis Details

The document needed to correctly unpack the TOF raw data is Ref. [21]. We use the abbreviations LE and TE to refer to Leading-edge data (in very-high-resn mode, 24.4 ps LSB) and Trailing-edge data (in high-resn mode, 97.6 ps LSB), respectively. The dynamic range is 21(19) bits in very-high-resn(high-resn) mode, or $\sim$51 μsec in both cases. The so-called DDLR values specify the data source: DDLR=1 means the TOFr5 tray, DDLR=2 means pVPD West, and DDLR=3 means pVPD East. For day 34 data and later, all three fibers are live and producing data. The TDIG boards are read out in the following order: 1, 0, 3, 2, 5, 4, 7, 6 - where TDIG 0 is closest to the η=0 end of the tray, and TDIG 7 is at the opposite end of the tray. TDIG boards 2 and 3 are masked out since the read-out from these boards was discovered to be dead after TOFr5 was installed. The INL tables were obtained from Ref. [22]. The mapping from TDIG board name to TDIG position numbers in the tray is given in Ref. [23]. Each INL file contains either 1024 values (for very-high-resn TDCs) or 256 values (for high-resn TDCs). The lowest 10(8) bits in a LE(TE) data word are the INL bin number, which is the first column in an INL file. The Float in the second column applies to the data word itself to remove the INL.

7.2 Basic Results

Applying the maps at the end of the fiber data format allows one to produce hit patterns versus the Tray detector channel (0-191), where channel 0 is the first pad on the first MRPC from the η=0 end, and 191 is the sixth pad on the 32^{nd} MRPC closest to the $\eta\sim$1 end. This hit pattern is shown in figure 57. In the top(bottom) frame is the number of LE(TE) data words versus the tray detector channel as the

black histograms. The periodic pattern of groups of 6 in this histogram is expected due to the sharing of signal inside the MRPCs for tracks near pad phi-boundaries. This pattern is a good indication that the maps in the fiber data format document are being correctly applied. The gap from 48 to 95 is from the two TDIG boards that were masked out of the data stream. There are 5 channels that are dead in both the LE and TE data (36, 108, 139, 156, and 180), due to a error in the electronic layout of this board.

The number of LE(TE) data words for which there was no accompanying TE(LE) word in the same event for the same detector channel are shown in the red histograms in the upper(lower) frames. This indicates that, in general, the matching of LE and TE words in the same detector channels in the same events is quite good. In the upper frame, there are approximately 9 k LE words per tray detector channel, and of these only some tens of these words were not accompanied by a TE word in the same detector channel (<<1%). The situation is somewhat less clean in the other direction. In the lower frame, one sees that a given TE hit is unaccompanied by a LE hit in the same channel at the 1% level. It therefore seems more appropriate to loop over LE hits and associate the TE data to the detector channels with LE data, rather than the other way around.

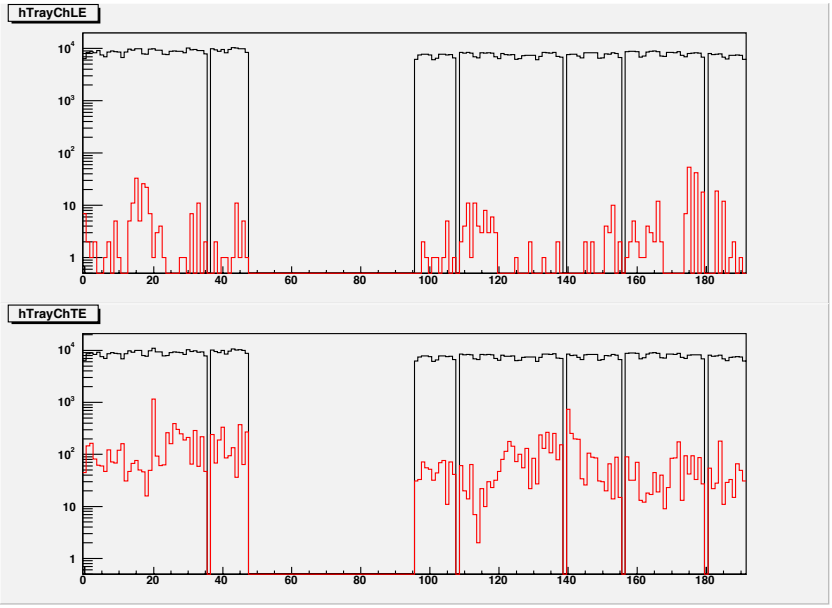


Figure 57: The LE and TE hit patterns versus the tray detector channel.

Now that it was clear that all the maps were being correctly applied, and that the LE and TE data match up well to each other in specific detector channels, it was time to start looking at the time stamps themselves. Events were selected in which there was exactly one valid time stamp for pVPD East detector channel 0 (12 o'clock) and exactly one valid time stamp for pVPD East detector channel 1 (4 o'clock).

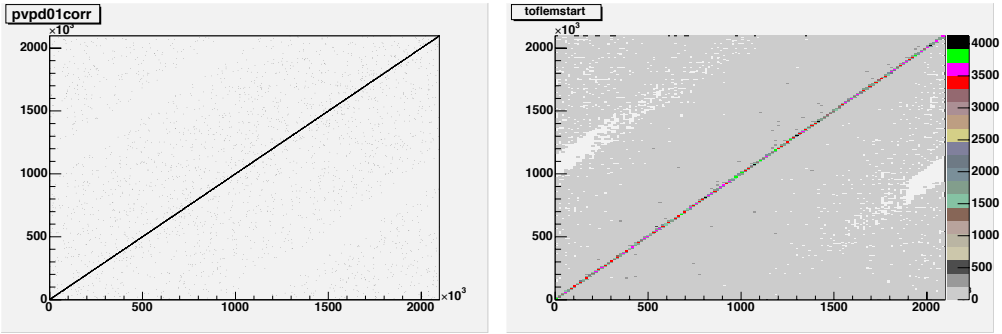


Figure 58: On the left, the correlation of the time stamps in two different pVPD detector channels in events in which there was one valid LE stop word for each detector channel, and on the right, the correlation of stop side time stamps with the start time calculated in the same event.

The difference between these two LE time stamps in the same event is shown on the left side in figure 58. Similar plots can be produced for any pair of pVPD detectors on the same side of STAR. The extremely strong band on the diagonal is a good indication that there is valid timing information in the raw TOFr5 data.

The event start time was obtained by averaging T_{east} and T_{west}, where each is the average over the accepted time stamps in each event on each side of STAR. A simple outlier rejection algorithm was required. The correlation of the event stop times from the TOFr5 tray to the start time so calculated from the pVPD is shown on the right side in figure 58. The axes span the entire 51 μsec dynamic range of the LE TDCs. Again, an extremely strong correlation along the diagonal is seen. The entire TOF physics program lives inside a tenth of each of the bins along the diagonal in this plot (each bin here is 400 ns wide).

The probability that a LE stop time stamp falls into a 73 ns-wide time slice relative to the event start time is shown versus the TOFr5 detector channel number in figure 59. The efficiency observed is ∼65-70%. This efficiency without the outlier rejection in the start-time calculation was lower, or ∼55%.

These simple results imply that the majority of the TOF Run-5 data words collected with the new clock-based TAMP/TDIG/TCPU approach on TOFr5 and both pVPD start detectors, and then read out using a new optical fiber electronics path and protocol, seems to give valid and sensible data. Most of the data words seem to be highly correlated with each other, even across fibers (start detectors versus MRPC stop detectors). About one-third of the stop side hits saved to the data stream are "out-of-time," due to the wide (∼25 μsec) trigger-matching windows used for the data analyzed above. This trigger matching window was, just later in the run, decreased to ∼5 μsec, and then decreased again to it's final value of ∼1 μsec. Our average data volume size with all three fibers active and wide matching windows in these minimum bias 200 GeV Cu+Cu data is <1 kB.

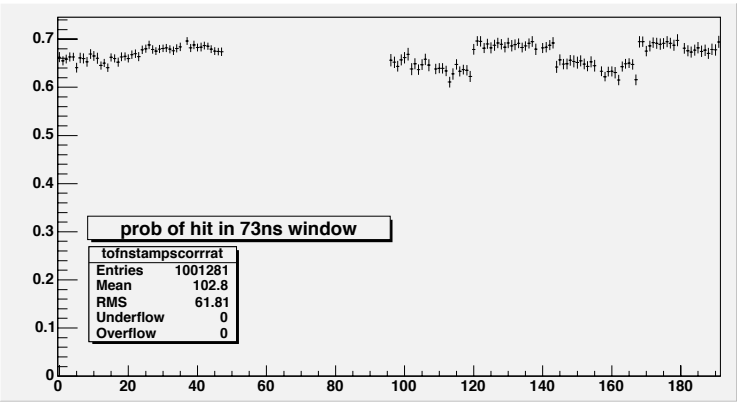


Figure 59: The fraction of the total number of stop-side LE data words that are contained within a 73 ns-wide window that begins(ends), event-by-event, 73 ns(146 ns) after the event start time (calculated using the start-side time stamps including outlier rejection).

7.3 INL

The INL correction was then read in and applied to all data words (all DDLRs). The HPTDC mapping was checked by filling two plots per HPTDC - one is the INL table read from the files of Ref. [22], and the other is the INL correction as it is applied as part of the event loop. In the former, the map INLfile→HPTDCnumber is hardwired based on Ref. [23]. In the latter, the INL bin number and HPTDC number is unpacked from the data word, and the HPTDC number is mapped onto the INL file number. The INL correction for this data word is then the INL value (from the file) for the given INL bin number.

To check that the INL values are being correctly applied to the data, the two INL curves (that read-in and that applied) are plotted versus the INL bin number (in a TH1F and a TProfile, respectively). A typical plot of this kind (there are 40 of these total), is shown in Figure 60. The INL corrections for a LE TDC (HPTDC=0) are on the left, and a TE TDC (HPTDC=3) on the right, versus the INL bin number. The black histogram is the table as read from the files, and the red points are the table as applied to the data during the event processing.

7.4 Start-side ToT

The next goals were to study the Time-Over-Threshold values, and look into the possibility that these might support a slewing-correction. The ToT distributions on the stop-side are of special interest, given the various approaches used on TOFr5 to address the MRPC/TAMP termination issues.

Studies of the stop-side ToT values and stop slewing corrections are described below. On the start side, however, the kinematics of the particles of interest are such

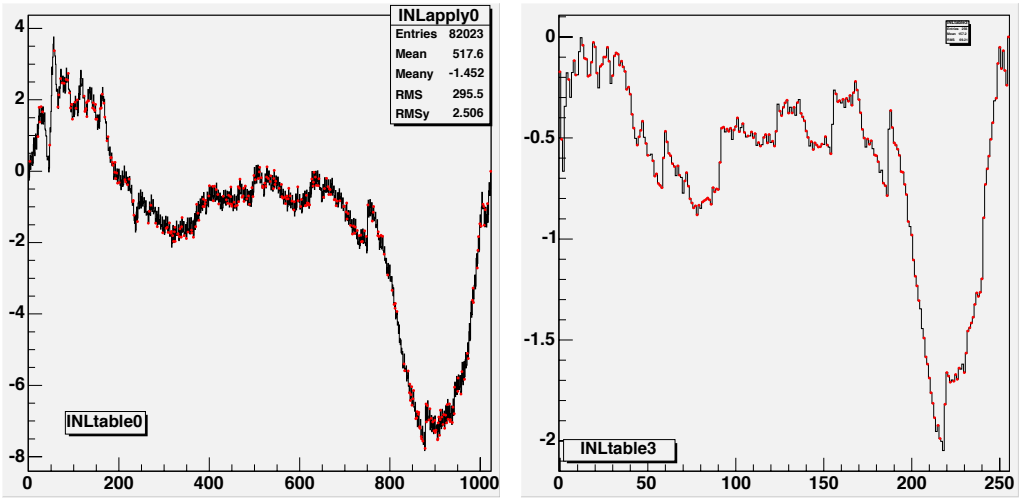


Figure 60: The INL corrections for a LE TDC (HPTDC=0) on the left, and for a TE TDC (HPTDC=3) on the right, versus the INL bin number. The black histogram is the table as read from the files, and the red points are the table as applied to the data during the event processing.

that direct measurements of the timing resolution of the system can be performed with the start-side data alone (no tracking or other STAR detector information is needed). This is an often underappreciated benefit of having a good start system that also uses the same electronics as is used on the stop side.

In the present Cu+Cu data, the pVPD is getting *lit up*, as it did in the previous Au+Au runs. In these previous runs the pVPD detectors regularly achieved a sub-50 ps resolution on the event start time (down to 24 ps in central Au+Au collisions). Thus, from the standpoint of the detectors themselves, the signals in the present Cu+Cu collisions are large and hence the detectors' contributions to the (start-)timing resolution is relatively small. We therefore expect a good start-timing resolution post-corrections in Cu+Cu. These detectors are exactly the same as in the previous runs, the only thing that has changed is the front-end, digitization, and read-out electronics.

The variable assumed to be related to the pulse height for the slewing correction in Run-5 is the Time-over-Threshold. This is `ToT = 4*te - le`, where `te` and `le` are the trailing- and leading- edge time values for a specific detector channel, respectively. The factor of four puts the trailing-edge data on the same time scale as the leading edge data - 0.0244 ns per INL-corrected time bin.[10]

Given the HV gain set in use on the pVPD and the fact that this is Cu+Cu, we expect the typical pVPD pulse heights are well above threshold. The ToT distribution one would expect would thus have a peak at some value well away from zero. Shown in figure 61 are the ToT distributions for the six pVPD start detectors - East(West) 1 through 3 are left to right across the top(bottom).

These show several of the expected trends. The trailing edge times *do trail* the

[10]The use of `ToT = te - le/4` and a time bin width of 0.0976 ns would be completely equivalent.

leading edge times in the same detector channel (ToT values are >0), as expected. Also, as expected based on the fact that the typical pulse heights are well above threshold, there are relatively few counts for "small" pulse widths, and the probability for specific pulse widths increases for increasing pulse widths, forming maxima for widths of 20-30 ns.

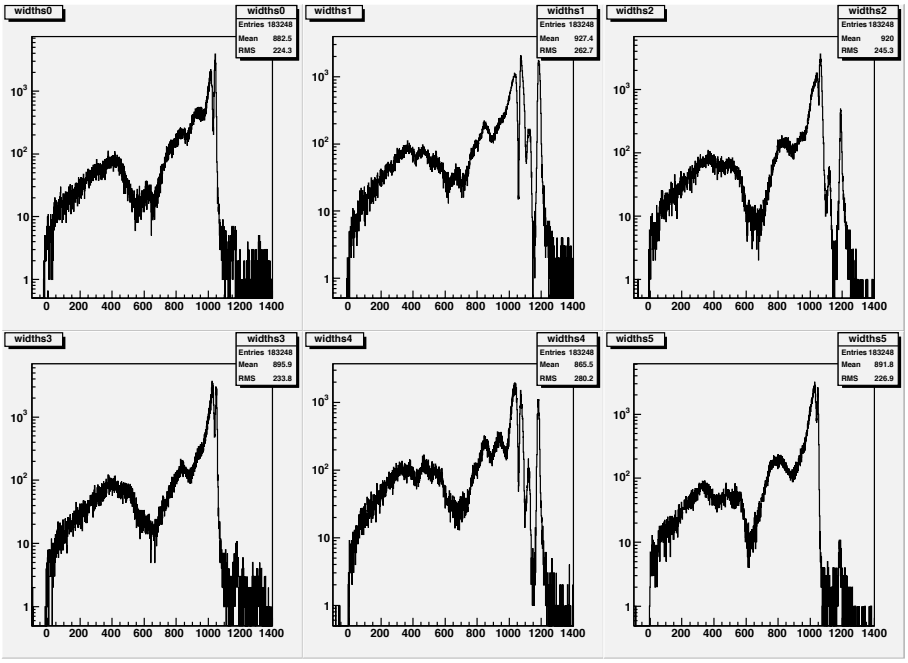


Figure 61: The ToT distributions for the six pVPD start detectors, East 1 is on the upper left and West 3 is on the lower right.

However, the shape of the distributions near these maxima is disturbing. One expects a distribution that tails off on both sides of some intermediate peak, but instead the distributions appear to cut-off for pulse widths larger than a maximum value of ∼25-27 ns. Each pVPD channel shows a certain number of sharp peaks immediately above these widths which were also not expected. These peak features (which occur in different numbers and at different time values in the different pVPD detector channels), and the apparent cut-off near ∼25-27 ns indicate a problem. We appear to be losing the ToT information for the largest pulses, which is unfortunate since it is these that lead to the best timing performance. These detector channels cannot be slew-corrected when the event's ToT values are in this strange upper region.

This ToT cut-off effect was interpreted as resulting from the input protection circuit on TPMT (the start-side's equivalent to TAMP on the stop side). Pulses that are larger than ∼4V fire this circuit, which cuts off the top of the pulse at this voltage but still passes the lower section of the pulse to the discrimination/digitization circuitry. However, when this circuit fires, it drops to zero impedance, which inverts & reflects the signal as it comes in. The reflected/inverted pulse then travels back up the signal pigtail cable (∼8.5 ft, ∼13 ns long), sees the large resistance of the PMT

base, and reflects again (but does not invert). After another ∼13 ns this inverted signal returns back to the front-end electronics, where it destructively interferes with (what is left of) the original signal. This drops the apparent pulse below threshold at this point, and hence cuts off the ToT values there. Twice the signal pigtail length is ∼26 ns, this is (up to small channel-dependent offsets) precisely the value of the ToT cut-off that is observed. We therefore installed 50 Ohm feed-through terminators at the pVPD PMTs at the first possible access.

Shown in figure 62 are the ToT distributions for the six pVPD detector channels following the addition of the terminators. Comparing this figure to figure 61, one notices immediately the distribution has much fewer "features" than the previous version - the high-cutoff and the addition peaks above this cut-off appear to be gone. The position of the most-probable ToT values dropped by a factor of ∼5, and are now near ∼225 very-high-resn bins, or ∼5.5 ns.

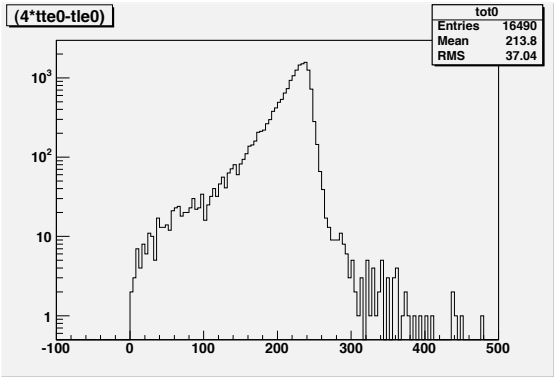


Figure 62: The ToT distributions for the six pVPD start detectors, East 1 is on the upper left and West 3 is on the lower right, following the addition of the terminators to the signal path.

7.5 Start-side Slewing

To avoid possible sources of bias, slew corrections of the start detectors typically study a time difference, or a difference of time averages, across different detector channels in the same event. The dependence of such a time difference on the slewing measure - previously the pulse area (ADC) now the pulse width (ToT) - is the direct measure of the pulse slewing effect and the best means to correct for it. When there are lots of hits (Au+Au or Cu+Cu), the most effective differences of time averages to use for a slew correction are the "1-<2>" difference, or the "<2>-<4>" difference.

The former requires all 3 detectors on one side to fire in the same event, the latter requires all six detectors fired. In both cases, the slewing correction functions obtained from these events can be applied to the same PMTs in all events. The "1-<2>" time difference can be formed on each side of STAR separately. The time difference of interest is the time from one detector minus the average of the two times

from the other two detectors on the same side in the same event. The latter forms the <2> average from one detector on each side of STAR (*e.g.* East 1 and West 1), while the <4> average is over the other 4 detectors (2 on each side) in the same event.

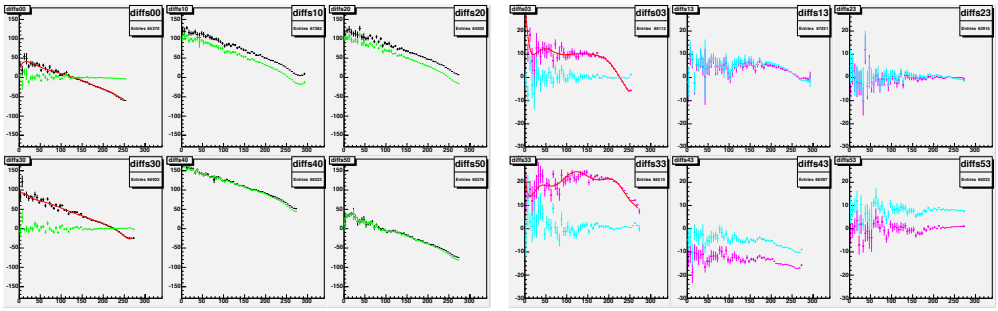


Figure 63: The start-slewing distributions versus the ToT for the six pVPD PMTs after start-calibration pass 0 (six left frames), and after pass 3 (right six frames), following the addition of the terminators to the signal path.

The left(right) six frames in figure 63 shows the slewing data and fits after the first(fourth) pass through the data. The vertical scales for the right frames were reduced by a factor of ∼6 relative to the left frames.

Following 12 passes through the data, the start resolution of the TOFr5 system following the addition of the terminators is shown in Figure 64. The timing resolution obtained - ∼57 ps (min.bias Cu+Cu) - is good, and consistent with that extracted from the data collected before the addition of the feedthrough terminators. The efficiency of the start correction increased (∼10%) with the addition of the terminators.

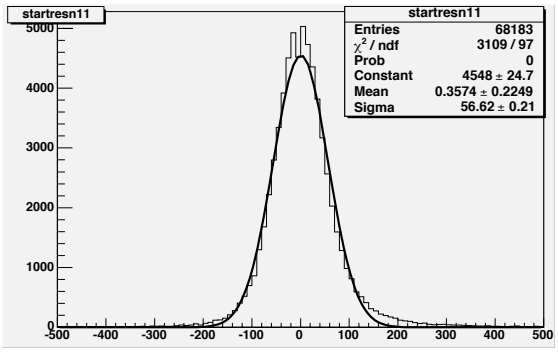


Figure 64: The start time resolution inferred from the "<2>-<4>" time difference distribution following the start-side slewing corrections for the the day 48 data (after the addition of the terminators). The abscissa is in units of picoseconds.

7.6 Stop-side Results

Once the STAR-tracking calibrations were in place, so-called "match trees" of the stop-side data could be produced. These contain the variables necessary to perform a preliminary stop-side calibration and make a first estimate of the total timing resolution of the TOFr5 system. In this section, there are a total of 633k(421k) matches available in the stop trees for the 200(62) GeV Cu+Cu data, respectively.

The start-side resolution as from the trees (using the same algorithm as described in section 7.5 above) is discussed in section 7.7. The TOFp-style stop correction approach was then applied in section 7.8 and the results are discussed in section 7.9.

7.7 Start-side corrections from the match trees

The start-timing correction discussed in section 7.5 above used local data that was collected early in the run when the HPTDC "trigger-matching" windows were very wide (25 μsec). The data for the present trees was only from that collected after the timing windows were reduced to $\sim$1 μsec.

The inclusive start-timing resolution obtained from the match trees for the 200 and 62 GeV data is shown in Figure 65. The resolution observed is approximately 51 ps and 83 ps, respectively, averaged over the full sample of minimum bias events available at each energy.

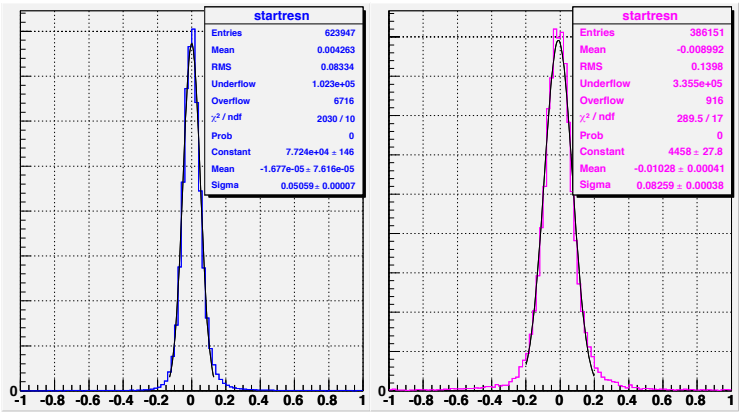


Figure 65: The start-timing resolution for the 200 GeV (blue) and the 62 GeV (magenta) Cu+Cu data from Run-5.

This value of $\sim$50 ps for the inclusive start resolution for the 200 GeV data is consistent with the estimates made using the Run-5 local data (see above). This was considered good at the time due to the unknown smearing to this quantity coming from the event centrality (these data are minimum-bias triggered by STAR). This smearing can now be exposed using the values of `nprimary` from the start trees. The start-timing resolution in nanoseconds versus nprimary is shown the the 200 GeV data in figure 66. This plot shows that the timing resolution in the most central

events is similar to that one gets by fitting just the core of the 1D plots (*e.g.* figure 65).

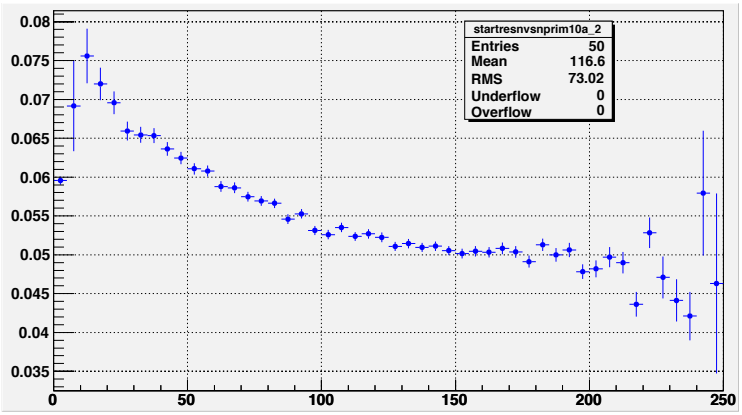


Figure 66: The start-timing resolution in nanoseconds versus nprimary for `indEvClass`=48 events at 200 GeV.

7.8 Stop-side corrections

The approach used here is the same as that used for the TOFp data from Run-2 [12]. This algorithm lives in $1/\beta$-space. This was chosen because the high-quality tracking information from the TPC defines a powerful "standard candle" in 1β-space for the TOF stop-side slewing and signal propagation time corrections. This standard candle is the track $1/\beta$ value, calculated initially and at any subsequent stage of the stop side calibrations, minus the $1/\beta$ value for the track calculated solely from the tracking information. One selects a sample of pions to determine the functions needed to remove the smearing from slewing and hit position, then applies these functions to all tracks in a subsequent pass through the data.

To get into $1/\beta$-space, the first thing needed is a crude timing offset in nanoseconds for each TOFr5 channel relative to the calibrated start time (also in ns) in the same event. The total timing resolution is so bad at this point that determining this initial offset only to ∼10% is perfectly sufficient. The mean path length in cm for all matches versus the TOFr5 channel number for the 200 GeV (blue) and the 62 GeV (magenta) Cu+Cu data is shown in the left frame of Figure 67. The low-(high-)eta end of the tray is on the left(right) side of the abscissa.

These average track-length values were tabulated for each MRPC module (32 total). In a subsequent pass through the data, these values of "`Savg`" were used to come up with a crude timing offset, "`preoffset`," via

```
timeraw = letime - tstart;
invbetaraw = vlight*timeraw/trklen;
preoffset = (Savg/vlight)*(1.-invbetaraw);
```

where `letime` is the HPTDC time stamp for this match in ns, `tstart` is the calibrated

start time (post start-ToT correction) in ns, `vlight` is 29.979 cm/ns, and `trklen` is the reconstructed total track length for this match obtained from the track reconstruction. The initial timing offsets extracted in this way are shown versus the TOFr5 channel number in the right frame of Figure 67.

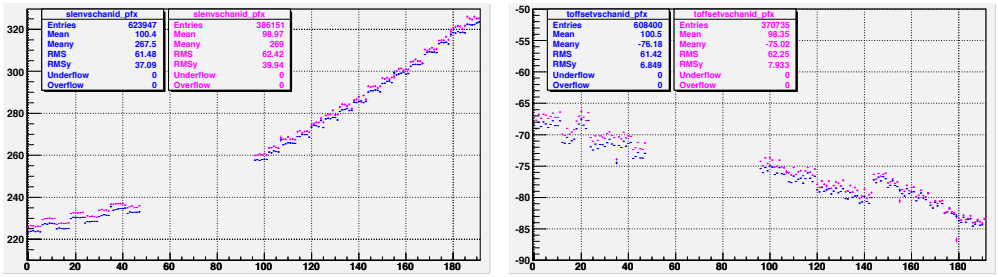


Figure 67: On the left, the mean path length, and on the right, the initial timing offsets, versus the channel number for the 200 GeV (blue) and the 62 GeV (magenta) Cu+Cu data from Run-5.

These crude timing offsets are used to jump immediately into $1/\beta$-space via

```
invbeta[0] = vlight*(timeraw + toffset[chanid])/trklen;
```

where `toffset[chanid]` is that shown on the right frame of figure 67 and `trklen` is the total path length for this track. All subsequent stop-side corrections and PID assignments thus also live in $1/\beta$-space.

7.8.1 Pion Selection

The pion selection method used here to select the matches to be used to extract the slewing and Zhit correction functions is now described. The mean TPC dE/dx (in keV/cm) for pions versus the momentum for the 200 GeV (blue) and the 62 GeV (magenta) data is shown in Figure 68. These mean values are used only as a (momentum-independent) consistency check on the pion selection done in $1/\beta$-space. The cut is loose (-0.6 keV/cm to +0.4 keV/cm relative to the pions), so the slight difference seen for the two beam energies is not so important.

The action is really occurring in figure 69. The Z-axis in this plot is on a logarithmic scale. In the upper left is the inverse velocity versus the momentum for all matches (with the only calibrations being the start correction and the definition of the crude channel-dependent offsets). The main peak is near 1 on the Y-axis since we chose offsets that insured this outcome. The upper right frame shows the matches defined as pions in the first calibrations pass through the data. In the two subsequent passes through the data (i.e. during the various slewing and Zhit calibration passes), the pion selection cut becomes tighter in $1/\beta$-space yet remains momentum-independent. The pion selection cut is set crudely in the first calibrations pass, is tightened twice in the next two calibration passes, and is then fixed for any subsequent passes.

The dE/dx mean values from figure 68 are used to set a pion consistency check above and beyond the $1/\beta$-space selection depicted in figure 69. The distribution

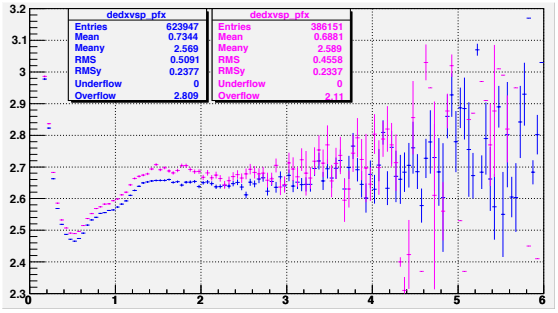


Figure 68: The mean TPC dE/dx (in keV/cm) versus the momentum for the 200 GeV (blue) and the 62 GeV (magenta) Cu+Cu data from Run-5.

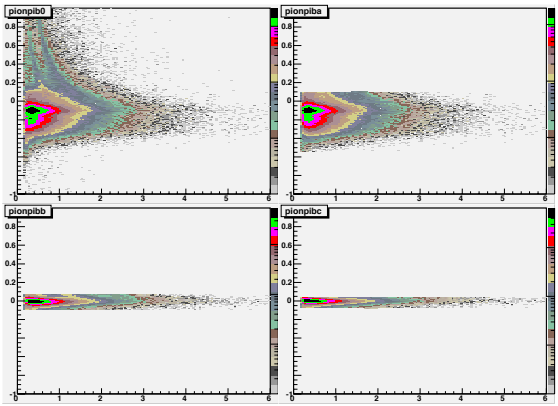


Figure 69: The values of $1/\beta$ versus the momentum for the first 4 passes. In the upper left is that for all matches after only the application of the crude timing offsets. The upper right shows those matches accepted as calibration pions for the first calibrations pass (over ToT, see below). The lower left(right) shows those matches accepted as calibration pions in the second(third) calibrations passes (over Zhit and ToT again respectively.

of TPC dE/dx values versus the momentum are shown in figure 70 for the same conditions used in figure 69. These could be named: all matches, bronze pions (pass 0), silver pions (pass 1), and gold pions (passes 2 and above) going from upper left to lower right.

7.8.2 ToT/Zhit fits

Matches flagged as calibration pions are used to fill specific TProfiles that will later be fit with a calibration function at the end of each pass. In the first calibrations pass, the quantity $1/\beta$-$1/\beta_{\mathrm{expected}}(pi)$ is plotted versus ToT for each TOFr5 readout channel. At the end of this pass, this distribution is fit with a polynomial for each channel and the fit parameters tabulated for use in subsequent passes. Examples of

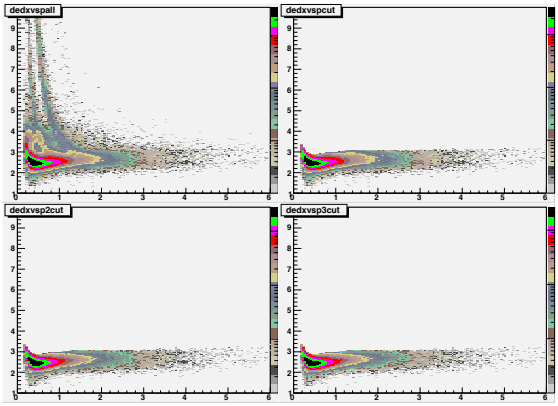


Figure 70: The TPC dE/dx values for the calibration pion selection. The individual frames correspond to the same calibration passes as seen in figure 69.

the ToT fits in this first calibrations pass are shown in the left frame of figure 71. One notices the quite different scales in ToT that exist in the different TDIG boards due to the different MRPC termination schemes employed at each location.

In the second calibrations pass, the ToT correction functions from the previous pass are applied, and new TProfiles are filled in order to attack the Zhit dependence. Examples of these Zhit fits are shown in the right frame of figure 71.

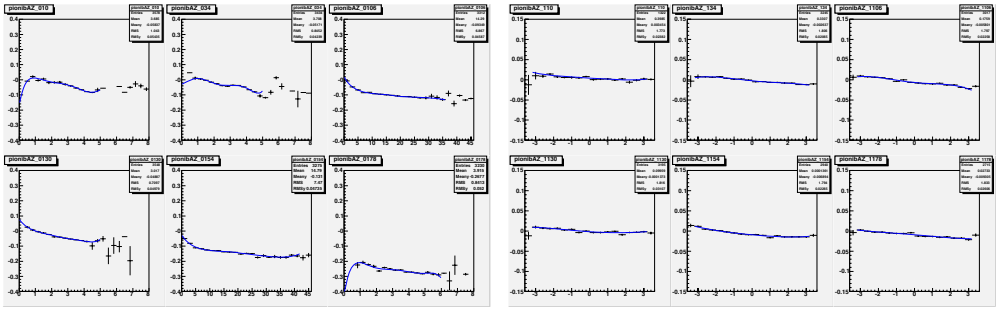


Figure 71: Examples of the ToT fits (left six frames) and (right six frames) performed after the first and second calibrations passes, respectively. Each set of six frames corresponds to one read-out channel from each of the six active TDIG boards on TOFr5 in the 200 GeV data.

The procedure continues in this way - ToT fit then Zhit fit then repeat - for 4 passes or so. A third pass is definitely necessary in this approach. Doing too many fit passes doesn't hurt. For the following results the procedure was stopped after 4 passes (two each over ToT and Zhit, respectively).

7.9 Total Resolution results

The stop-side calibrations are complete at this stage. To quote a timing resolution in ns, the $1/\beta - 1/\beta_{\text{expected}}$(pi) distributions are converted to a time scale via

`timelike = savgModule[kModule]*(1/`β`-1/`β_{expected}`(pi))/vlight.`

These distributions are then fit with Gaussians. The total timing resolution versus the TOFr5 channel number thus extracted is shown for the 200 and 62 GeV data in figure 72.

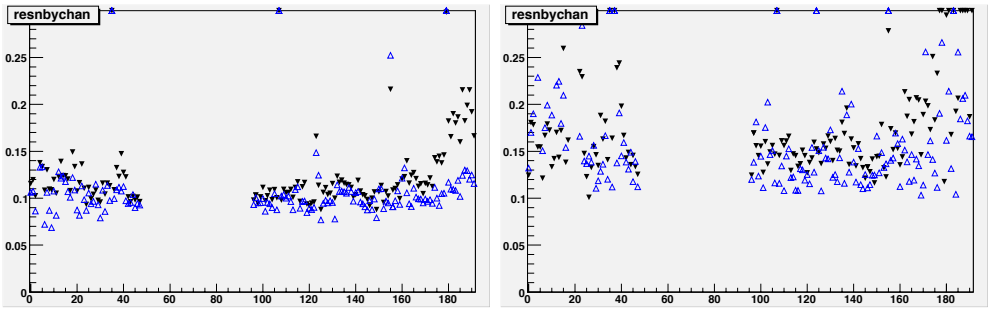


Figure 72: On the left(right), the total timing resolution for the 200(62) GeV Cu+Cu data from Run-5 versus the TOFr5 channel number. The black points are for all calibration pions while the open points are for a specific set of golden track and match match cuts (described below).

The histograms of these timing resolution numbers over all active read-out channels are shown in the figure 73. The timing resolution histogram for all matches in the 200 and 62 GeV data is shown in the two left frames. The total resolution observed is of order 108(151) ps over 144 channels at 200 and 62 GeV. The timing resolution histogram for "golden" matches (described below) in the 200 and 62 GeV data is shown in the two right frames of in Figure 73. The total resolution observed for these matches is of order 100(137) ps over 144 channels at 200 and 62 GeV.

The cuts used to select "golden" matches are defined by the plots shown in figure 74. The standard deviation of $1/\beta$-$1/\beta_{\rm expected}$(pi) for matches with $0.5<p<1.5$ GeV/c is plotted versus the track global dca (upper left), the number of primaries (upper right), $Z_{\rm vtx}$ (lower left), and η (lower right). One sees tracks with dca>1.5 cm, and events with —$Z_{\rm vtx}$—>30 or so have a relatively poorer time resolution. Tracks with less than ∼30 hit points also have a poorer time resolution. The cut used here to define golden matches was thus

$Z_{\rm vtx} > -10$
$Z_{\rm vtx} < 30$
nfitpoints >= 30
dca < 1.5

The PID capabilities over all active read-out channels are indicated in figure 75. In both the left and right sets of four frames, the TPC dE/dx is shown versus the momentum in the upper left for all tracks with $1/\beta<1.03$. The upper right through lower right plots in each set of four frames show $1/\beta-1/\beta_{expected}$ versus the momentum for pions, Kaons, and protons, respectively. In all eight plots, the Z-axis is logarithmic.

These same data have also been calibrated using a different strategy. The main difference to that done above is in the pion selection, where instead of a momentum–independent cut in $1/\beta$-space, a tight momentum cut is placed at a low momentum (∼0.3-0.6 GeV/c) where the dE/dx information from the TPC still provides good pion PID. Figure 76 shows the total timing resolutions for each TOFr5 channel from this approach for the Cu+Cu data at 200 GeV (left frame) and 62 GeV (right frame). The ultimate timing resolution obtained from the two calibrations approaches is consistent.

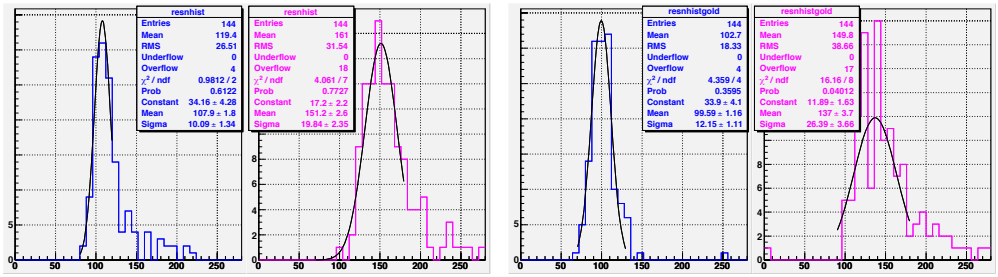


Figure 73: In the two left frames, the histograms of calibrated timing resolutions across all active TOFr5 read-out channels for the 200 GeV (blue) and the 62 GeV (magenta) Cu+Cu data from Run-5. The two right frames depict the average total time resolution of TOFr5 following additional "golden track" cuts.

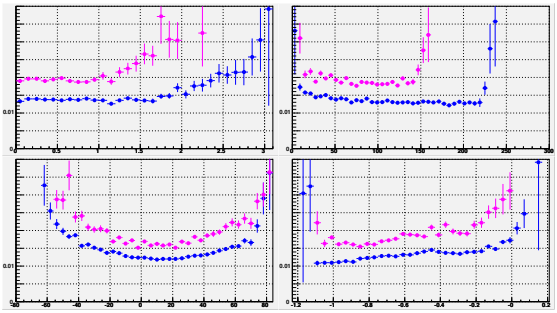


Figure 74: The standard deviation of $1/\beta$-$1/\beta_{expected}$(pi) for matches with $0.5<p<1.5$ GeV/c following all start and stop corrections versus the track's global dca (upper left), the number of primaries (upper right), $Z_{\rm vtx}$ (lower left), and η (lower right).

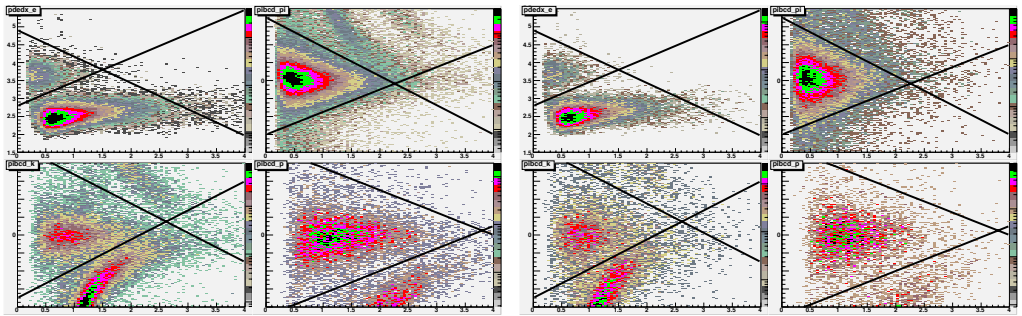


Figure 75: In the left(right) four frames, the PID distributions in $1/\beta$-space for electrons (upper left) through protons (lower right) in the calibrated 200(62) GeV data.

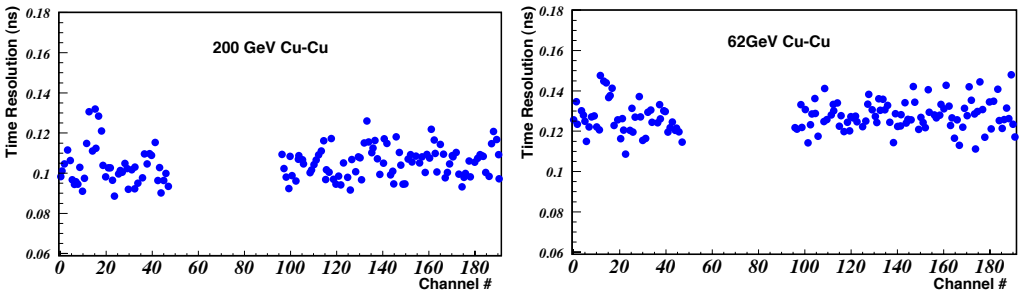


Figure 76: In the left(right) frames, the total timing resolution obtained from an alternate calibration algorithm for the 200(62) GeV Cu+Cu data from Run-5.

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