STAR Time-of-Flight
Capital Equipment Proposal
Clock Upgrade Project

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1 Overview

The STAR Collaboration has just successfully completed the large-area time-of-flight (TOF) construction project. The proposal and update material, management plan, closeout report, and final review report may be found at
http://www.bonner.rice.edu/~eppley/TOF_proposal_20040524.pdf
http://www.bonner.rice.edu/~eppley/Technical_design_update_20050816.pdf
http://www.bonner.rice.edu/~eppley/TOF_management_plan_Dec20_2005.pdf
http://www.bonner.rice.edu/~eppley/STAR_TOF_closeout_report.pdf
http://www.bonner.rice.edu/~eppley/STAR_TOF_final_review_report.pdf

The commissioning of the 70% of the system installed for Run 9 went exceptionally smoothly. We anticipate that the commissioning of the full system in Run 10 will go smoothly as well. This new detector approximately doubles the percentage of identified charged hadronic particles to 95% of those produced within its acceptance. This will allow STAR to extract the maximum amount of information available for measurements on an event-by-event basis.

A final DOE review of the TOF project held at BNL in August 2009 found that the project had met all the deliverable and performance requirements. In particular, the average channel of TOF electronics adds an uncertainty of ~25 ps to the timing measurement exceeding the requirement of 45 ps. The system as a whole is expected to provide a timing measure with 80-85 ps accuracy in AuAu collisions, exceeding the requirement of 100 ps.

2 Scope of work

The STAR TOF electronics runs on a 40 MHz clock produced by a single oscillator located on one of the four *THUB* cards, designated the master *THUB*. The clock and the associated clock reset signal are distributed from the master *THUB* to the three slave *THUBs* over RG58 coaxial cable. The signals are transmitted differentially with the clock on one pair of coax and the reset signal on another pair. The clock and reset signals are transmitted from the *THUBs* to the HPTDC chips on the readout *TDIG* cards on 120 trays and two start electronics assemblies. There are a total of 2910 HPTDC chips. Each HPTDC chip keeps its own local time using a 21-bit, 51 μs, counter. There are in effect 2910 independent time zones in the TOF system. The phase difference between the HPTDC chips is learned from the data. This phase difference between HPTDC chips must remain stable over substantial time periods for the TOF system to produce useful results with the required timing precision.

The signal propagation time in coaxial cable is known to vary with temperature. Ted Nussbaum has evaluated the clock distribution cables used in the TOF system and found an 12 ps timing shift per 80 ft. of cable per degree F. The longest clock cable in the TOF system is ~120 ft. so we could expect a ~18 ps phase shift between different quadrants of

the TOF system per degree F of temperature change. The air temperature in the STAR collision hall is stable to about 2 F. This variation, if uncorrected, could degrade the timing resolution from 80 ps to 90 ps.

A simple solution to this potential problem is to have the clock distributed from a central point so that the clock distribution cables are all the same length. With that topology, shifts in air temperature should cancel to the extent that the temperature shifts are uniform within the collision hall. A further benefit of building a central TOF clock or *TOCK* card will be to allow the expansion of the system to more than four *THUB* cards, the current limit. This expansion is necessary to enable adding a TOF-based muon detector (MTD) to STAR. The MTD will require the same clock as the TOF system since it will use the same start detector.

The *TOCK* card will be installed in a chassis in rack 1B1 or 1B2. It can be powered by a spare Wiener LV channel or by a simple "brick" on a network power switch outlet. We plan to use cat-6 cable to distribute the clock and resets to the *THUBs*, identical to the cable now used between the *THUBs* and the TOF trays. The cat-6 cable is more than 50% less sensitive to temperature change (5 ps per 80 ft. per degree F) compared to the coax, but it is somewhat more sensitive to changes in position. The *TOCK* card will have eight outputs. It will have an MCU and CANbus connection but can be operated without CANbus if desired. The reset signal will still be generated by a master *THUB* that will use its connections to daq, trigger, the TOF electronics monitor, and the TOF control pc to decide when resets are issued. The master *THUB* will send a reset signal to the *TOCK* card which will fanout the signal into up to eight outputs distribute

The anticipated time period for this upgrade project is October 1, 2009 to December 31, 2010. Following tests of the completed card at Rice and UT, we plan to install and test the *TOCK* card at STAR during the Run 10 – Run 11 shutdown interval. The *TOCK* card design will be reviewed by the same team that reviewed all TOF project electronics. It will include Jo Schambach and Lloyd Bridges.

Rice University physicists G. Eppley, F. Geurts, and W.J. Llope will actively participate in this upgrade to the TOF detector. Electronics design and testing is done in collaboration with J. Schambach at UT Austin. There are a number of Rice undergraduate students, employed during the summer term, as well as graduate students who participate in TOF data analysis.

3 Deliverables, Costs

(Amounts in k$.)

Design, test, and install *TOCK* board	$51.5
PC board production (10)	2.2
PC board assembly (8)	2.2
PC board contingency	3.0
Components	3.3
Clock distribution cables, chassis, power	2.4
Shipping, laboratory supplies	0.8
Travel (4 trips to BNL)	8.1
Total	$73.5

The item “Design, test, and install *TOCK* board” anticipates using Rice engineers and the costs are fully burdened. The estimate is based on 0.4 FTE for Ted Nussbaum. The “Shipping, laboratory supplies” cost includes an overhead of 52.5%. Travel cost includes an overhead of 26%. Personnel receive a per diem allowance of $35 for domestic travel. Material purchases and outside fabrication do not receive a burden from Rice.

The PC board contingency covers the case where the board would require modification after the first prototype is built.