STAR-TOFp System Test I

STAR-TOFp Group

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Abstract

The TOFp proposal was reviewed during a phone conference on December 15, 1998, and in meetings at the January 1999 collaboration meeting. The revised report from the review committee, received April 13, 1999, confirmed the need for the proposed "System Test" of particular custom electronics. The STAR spokesman has requested a separate document that describes the specific goals and the funding necessary for this effort. This is that document. We look forward to any comments. This effort is ready to begin immediately after the requested funds are made available.

1 Overview

According to the original TOFp proposal, [1] two system tests were planned as part of the TOFp construction effort. This first of these ("TOFp SysTest-I") was proposed to concentrate on the "In-Tray" components, while the second ("TOFp SysTest-II") was to concentrate on the TOFp system as a whole including the DAQ and slow controls interfaces. The TOFp review committee agreed with this plan, but recommended that funding for the project as a whole be postponed until successful completion of SysTest-I. In this document we describe briefly the specific plans and costs to perform SysTest-I. We note that it is sensible to include in SysTest-I the testing of specific aspects of the system originally planned for SysTest-II, as described below. We refer the reader to the TOFp proposal, and to a recent TOFp plenary talk, [2] for the details on the system and its implementation in STAR, as proposed.

There are a number of primary and secondary goals of the TOFp SysTest-I. The primary goals include:

1. Prove functionality and stability of the proposed Cockroft-Walton bases,
2. Prove functionality for fast timing and stability of the proposed in-tray discriminators,
3. Prove appropriateness of "Flat-Coax" signal cable,

while the secondary goals include:

1. Develop experience with the Slow Controls interface.

Each primary goal is reached via a number of specific measurements that are outlined in section 2 below. Once the necessary funding is received, the fabrication of the custom electronics and the collection of the bench data is expected to take approximately two months in total. At this point it is our understanding that the test results are to be reviewed by the TOFp Review Committee to determine if the TOFp construction effort is to be funded.

To accomplish the goals above, the equipment seen in Figure 1 must be assembled. The reasoning leading to particular aspects of this design of the test setup is outlined below. The items written in italics are to be purchased or fabricated as part of this effort, while the other items shown are already in house and are now dedicated to this project. Hence the items labelled in italics incur costs (equipment only), which are described in detail in section 3 below. Funding for these components is needed before SysTest-I can begin. The manpower needed for the project management, the electronics engineering, and the testing itself are also already in place.

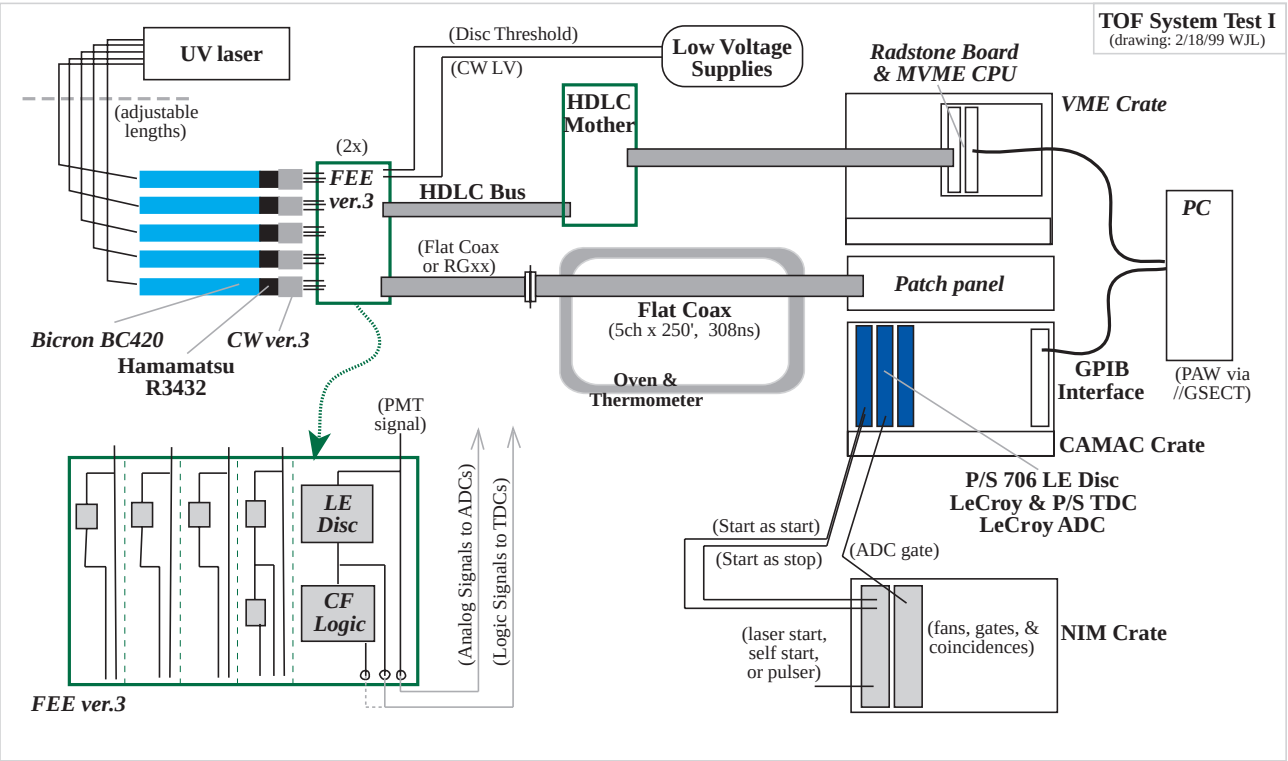

Figure 1: A schematic of the equipment to be used for the presently proposed TOFp System Test. The items written in italics are to be purchased or fabricated as part of this effort. All other items and the necessary manpower are already in place.

Before listing the specific tests to be performed, some introductory comments are necessary.

1. **Radioactive source** *vs.* **cosmics** *vs.* **laser**
   The (2cm) thickness of the TOFp slats and the thickness of trigger slats rules out the use of available radioactive sources to provide the scintillator pulses to test this system. Cosmic rays are the next option. The 80.2 ps/cm propagation delay of the scintillation light in the slats requires one to constrain the location of the hits to <1 cm^2. As five slats are to be exercised in SysTest-I, this implies that <1 cm^2 cosmic trigger slats are needed - one above and one below the "stack" of TOFp slats to be tested. This limits the rate of cosmics satisfying the trigger condition to much less than 1/minute, which is too small to reasonably perform these tests. Thus, the only viable option to provide the scintillation signals needed for these tests is a UV laser, which is in house and dedicated to this effort. The same laser was used for recent similar fast-timing studies. [3]

2. **Cable tests**
   In specific cases, the performance of "Flat-Coax" cable proposed for carrying the signal cables to the platform will be checked versus the manufacturers specifications. In all other cases, it will be compared to the performance of RG58 coaxial cable of the same length. Please note that we are not implying *a priori* that we expect the flat coax to outperform a (larger) bundle of RG58 in every respect. Indeed, the goal of these tests is rather to understand the performance of the flat coax cable in detail and to decide if its (primarily mechanical) benefits are outweighed by any significant performance degradation.

3. **In-tray Discriminator**
   A primary goal of this test is to prove again the functionality of the proposed in-tray discriminator. The present version (v.II) is Leading Edge (LE) and has been shown to have a rise time $<$1ns and a jitter on the order of 10ps. Two copies of the 5ch Disc/CWcontrol boards will be built for this test. In each board, each of the channels is the same LE discriminator described in the proposal. In two channels in each board, additional electronic logic will be added to make the equivalent of Constant Fraction (CF) discriminators for these channels. For these channels, this logic can be bypassed trivially, as shown in Figure 1. On the basis of experience we expect that LE discrimination is more appropriate for the present system than CF. However, this plan allows us to test up to 4 slat assemblies with the initial discrimination being CF to confirm this expectation for the present system.

4. **Controls**
   All of the primary goals of SysTest-I are satisfied with a simple CW control and discriminator interface (*i.e.* the "blue box"), which exists, and a low voltage supply, which exists. However, a secondary goal of SysTest-I involves exercising the slow controls interface. Thus, each Disc/CWcontrol board will be built to accept the (existing) simple interface for the CW control and level setting, as well as via the HDLC bus from the (existing) mother and mezzanine boards.

2 SysTest-I Measurements.

Here list specific measurements to be made. For each, we list the goal of the measurement, the method, and the result to be obtained. It is important to recognize that the test setup shown in Figure 1 is, in all but a trivial aspects, exactly the same as the proposed implementation of the TOFp system in STAR, except on a smaller scale.

1. **CW: Functionality**

   (a) *Goal*
   Prove CW version III provides high voltage to PMTs.

   (b) *Method*
   Construct five (5) such bases and use throughout SysTest-I.

   (c) *Result*
   Show expected signals from PMTs.

2. **CW: Stability**

   (a) *Goal*
   Prove CW version III is stable over long periods.

   (b) *Method*
   Construct five (5) such bases and use throughout SysTest-I.

   (c) *Result*
   Show CW version III is stable over long periods.

3. **Discriminator: Functionality**

   (a) *Goal*
   Repackage in-tray discriminator version II into final board layout and remeasure performance.

   (b) *Method*
   Show fast timing performance by measuring variance of time difference distributions between different TOFp slats under varying conditions of pulse height and position on slat, discriminator thresholds, temperature, and so on.

   (c) *Result*
   Variance of time difference distributions between different TOFp slats subject to a variety of variables.

4. **Flat-Coax Cable: Jitter**

   (a) *Goal*
   Investigate intrinsic jitter in flat-coax cable.

(b) *Method*
Split pulser signals and measure cable jitter and compare to RG58 coaxial cable.

(c) *Result*
Intrinsic cable jitter in picoseconds.

5. **Flat-Coax Cable: Cross talk**

(a) *Goal*
Investigate cross talk between neighboring channels in flat-coax cable.

(b) *Method*
Split pulser, PMT, and discriminator signals and measure line shape and magnitude of signals in neighboring channels versus the input signal rise time, magnitude, and rate.

(c) *Result*
Measurement of neighboring channel attenuation in dB and comparison to manufacturers specs. Also measurement of lineshapes for both analog and logic signals in neighboring channels.

6. **Flat-Coax Cable: Area Attenuation, analog signals**

(a) *Goal*
Investigate flat-coax area attenuation for analog signals.

(b) *Method*
Measure ADC distributions for PMT signals after flat-coax and ADC distributions for PMT signals after RG58 or the same length.

(c) *Result*
Comparison of ADC distributions for PMT signals following flat-coax and those following RG58.

7. **Flat-Coax Cable: Rise Time Attenuation, logic signals**

(a) *Goal*
Investigate flat-coax rise time attenuation for logic signals.

(b) *Method*
Measure 20%-80% rise time for logic signals after flat-coax versus the input signal rise time, magnitude, and rate and compare to same quantities for RG58.

(c) *Result*
Dependence of output rise times versus input logic signal parameters after flat-coax and comparisons to RG58 of the same length.

8. **Flat-Coax Cable: temperature dependence**

(a) *Goal*
Measure temperature dependence of cable properties.

(b) *Method*
Put most of cable in an existing oven.

(c) *Result*
Signal properties versus the temperature from ∼70 to ∼110 °F.

3 SysTest-I Costs.

In this section, we tabulate the costs for SysTest-I. These efforts will begin immediately after the receipt of these funds, and are expected to take approximately two months. All costs are actual, not estimates. There are no labor costs.

ITEM	QUANTITY	EQUIPMENT ($)
BC420 slats	5	800
Kinetics 1992	1	730
Kinetics 3516	1	4,100
HP L.V. Supply 1-U	1	900
PC/Xceed/EPICS	1	1,500
Patch Panel	1	
Hardware		100
Connectors		500
HVSys Bases		
Development†		800
Prototypes‡	6	570
Final‡	50	3,750
FEE v.4 Board	2	
PCB Drop Charge		500
PCB Components		2,700
FEE v.5 Board	2	
PCB Drop Charge		500
PCB Components		2,700
Total		**20,150**

† This development was performed out of house, and hence appears as an equipment cost for this item.
‡ Cost per cell in prototype round is 95$ for 6 cells, while the cost per cell for the final production of 50 is 75$ per cell.

References

[1] http://bonner-mac8.rice.edu/~TOFp/default.html

[2] http://bonner-mac8.rice.edu/~Spectra/From_99_February/Llope/

[3] S. Ahmad *et al.*, Nucl. Inst. Methods A, **400**, 149 (1997).