



# MRPC Time Of Flight Development

*W.J. Llope for the STAR TOF Group  
RHIC Detector Advisory Committee Meeting  
Dec 19-20, 2002 BNL*

## Outline

- Role of Upgrade needing this R&D, performance specification
- Experimental verification of the approach
- The Multigap Resisitive Plate Chamber (MRPC) technology
- Performance & viability for use in STAR
- Major technical challenge: the electronics
- Proposed R&D on MRPC electronics
- Manpower, Milestones, Deliverables

0 0.2 0.4 0.6 0.8 1 1.2 1.4  
mass (GeV)

# STAR TOF COLLABORATION

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The goal is to cover the entire cylindrical surface of the STAR TPC  
with an inexpensive but high-performance Time Of Flight system, “STAR TOF”

Proposal for the construction project is in late stages of review within the STAR Collaboration

Aiming to start building in the beginning of FY04, ready to take data 12/15/2005...

Goal/Role: Charged hadron particle identification (PID) over full cylindrical surface of STAR TPC

Requirement: Total system time interval resolution of **100ps or better**.

$$100\text{ps} \geq \sigma_{\text{start}} \oplus \sigma_{\text{stop}}$$

$$\rightarrow \sigma_{\text{start}} < \sim 50\text{ps}$$

$$\rightarrow \sigma_{\text{stop}} < \sim 86\text{ps}$$

$$\sigma_{\text{start}} = \sigma_{\text{startdet}} \oplus \sigma_{\text{elect}} \oplus \sigma_{\text{startcorr}}$$

$$\sigma_{\text{stop}} = \sigma_{\text{mrpc}} \oplus \sigma_{\text{elect}} \oplus \sigma_{\text{stopcorr}}$$

from test beams (test FEE, camac digitization)

$$\sigma_{\text{mrpc}} \oplus \sigma_{\text{elect}} \oplus \sigma_{\text{stopcorr}} \sim 60\text{-}70\text{ps}$$

$$\sigma_{\text{mrpc}} \quad \sim 54\text{ps}$$

$$\sigma_{\text{elect}} \quad \sim 40\text{ps}$$

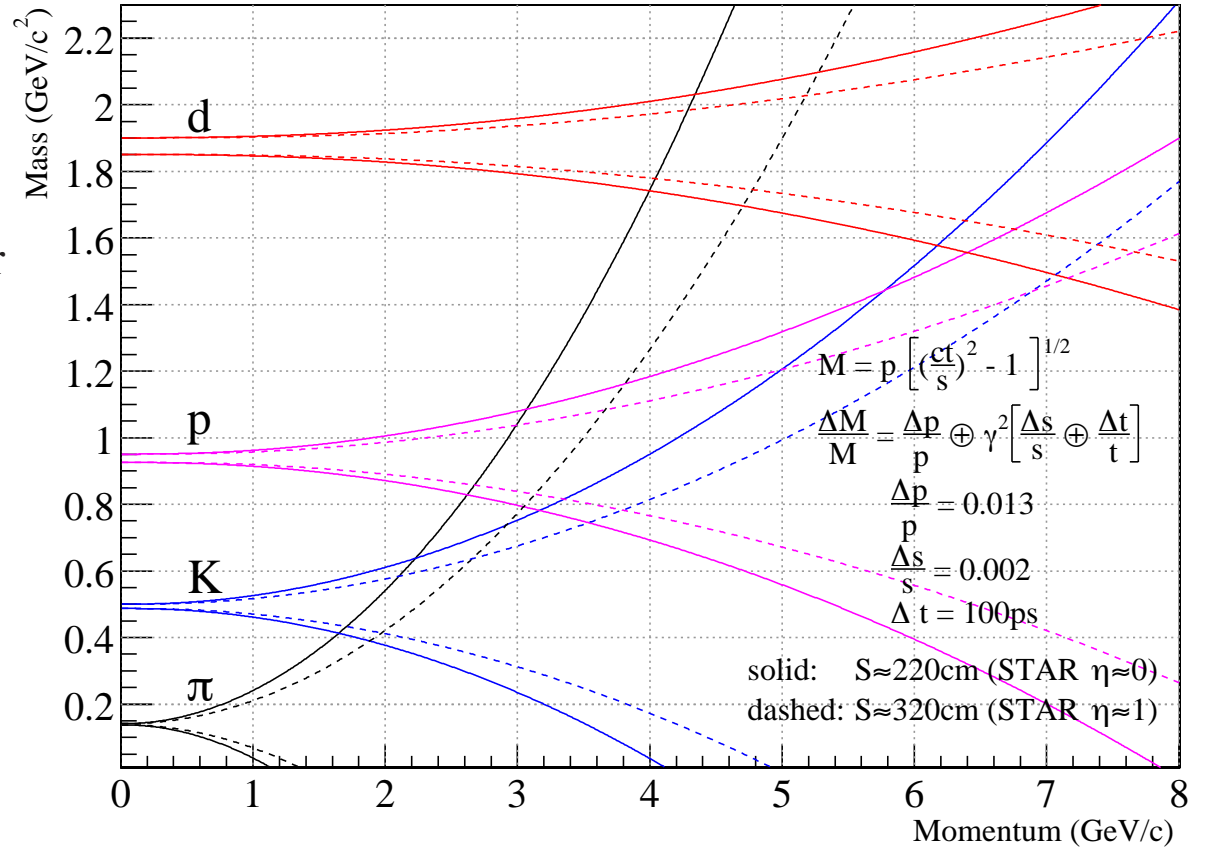
$$\sigma_{\text{stopcorr}} \quad \sim 20\text{ps}$$

Goals of present R&D focussed on development of front-end and digitization electronics that meets this level of performance...

expected momentum limits for direct PID...

$2\sigma$ PID	TPC dE/dx	TOF ( $\eta \sim 0$ )	TOF ( $\eta \sim 1$ )
$\pi/K/p$	$\sim 0.7$ GeV/c	$\sim 1.6$ GeV/c	$\sim 2.0$ GeV/c
$(\pi+K)/p$	$\sim 1.0$ GeV/c	$\sim 2.6$ GeV/c	$\sim 3.2$ GeV/c
d	$\sim 1.0$ GeV/c	$\sim 4.0$ GeV/c	$\sim 4.7$ GeV/c

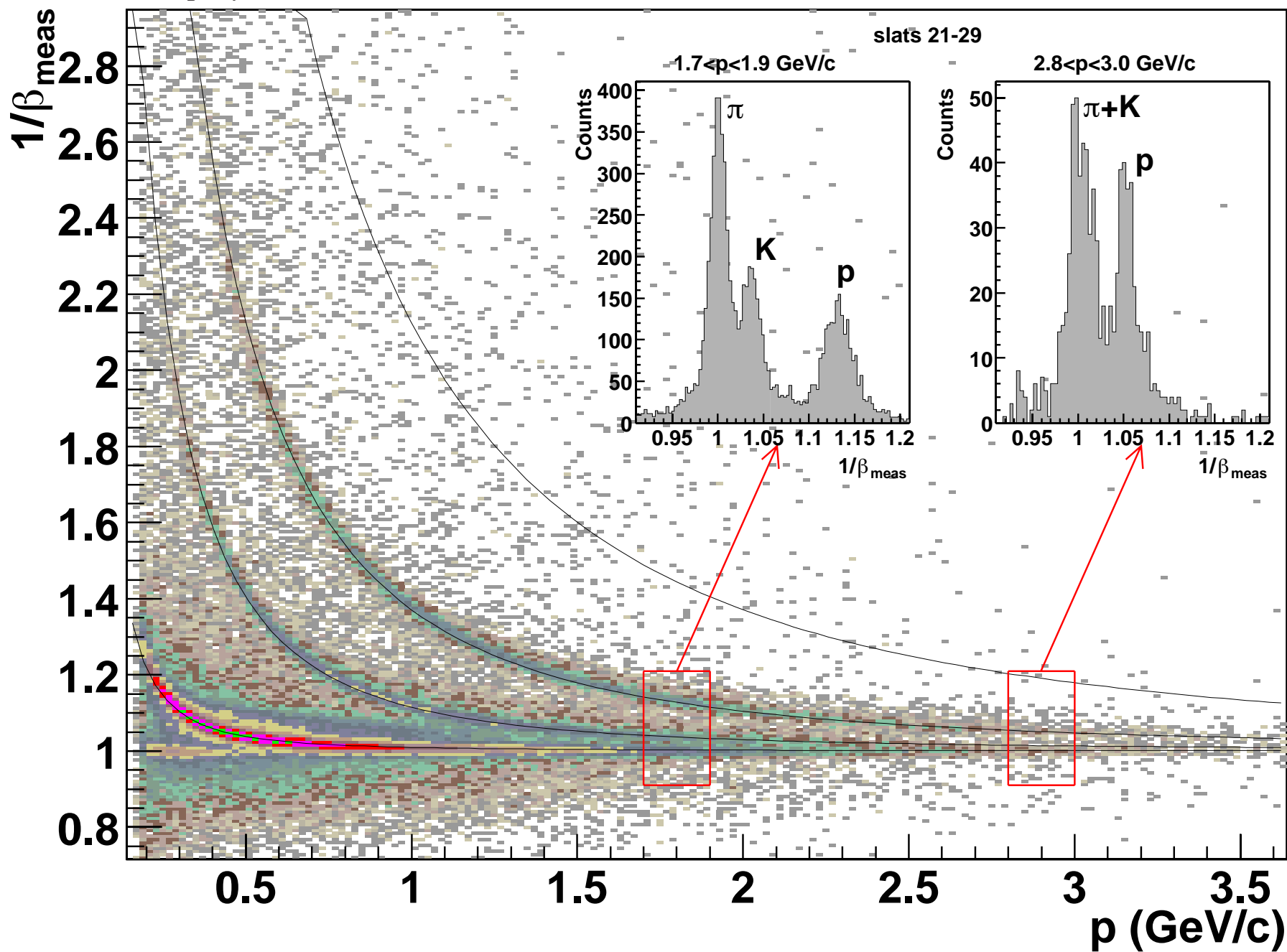
dedx: PID over **<50%** of pT spectra, soft  
 tof(+dedx): **>95%**, harder



experimental verification of the TOF approach in  $\star$  comes from the **TOFp** systems (TOFp+pVPD)...

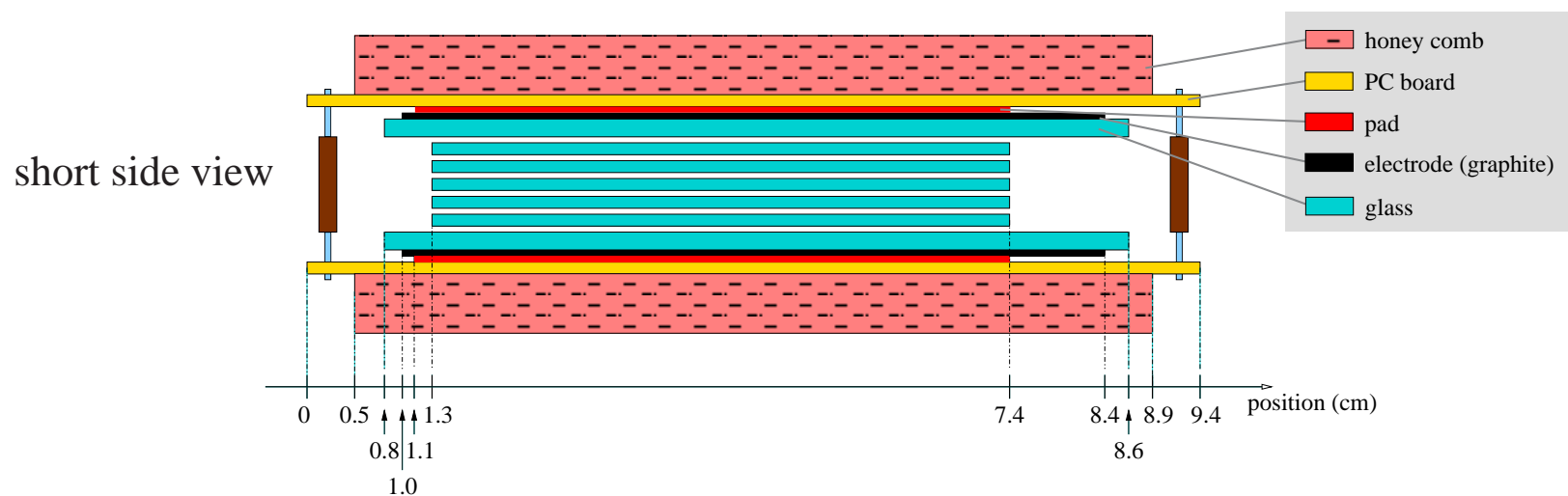
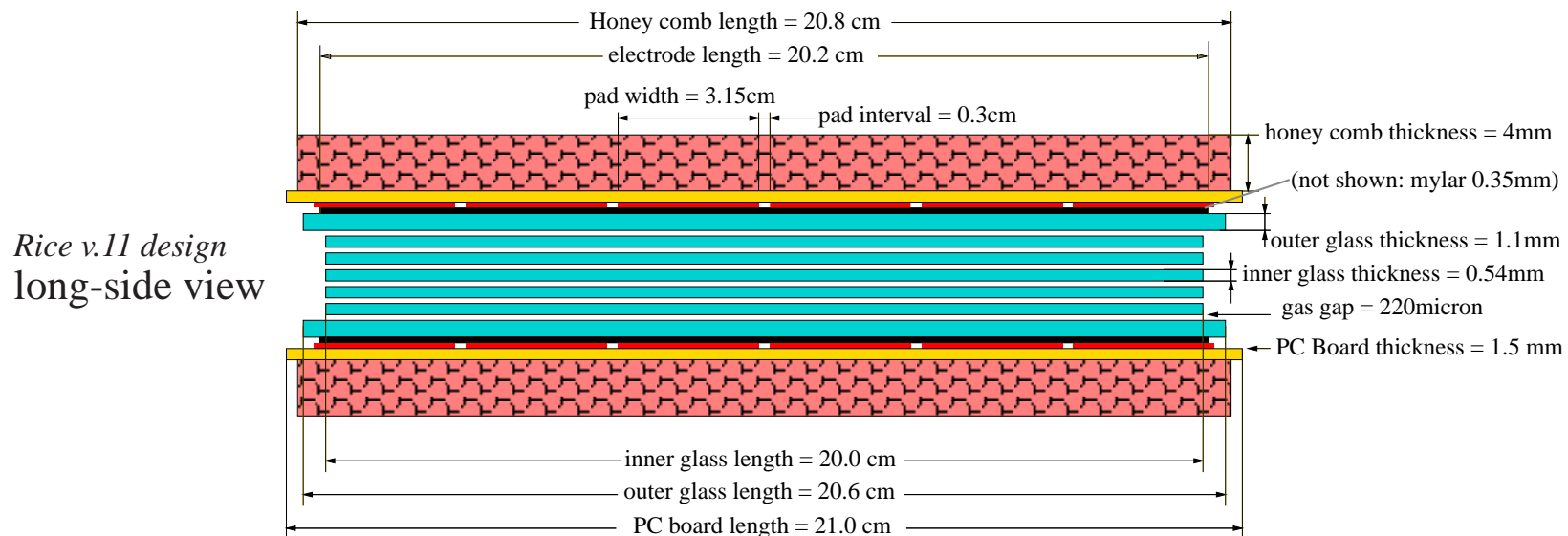
(not MRPCs...  
...similar  $\sigma_t$ )

*TOFp Systems, RHIC Run II, 200 GeV,  $\sim 0.9M$  STAR central events*



## Multigap Resistive Plate Chambers (MRPCs)

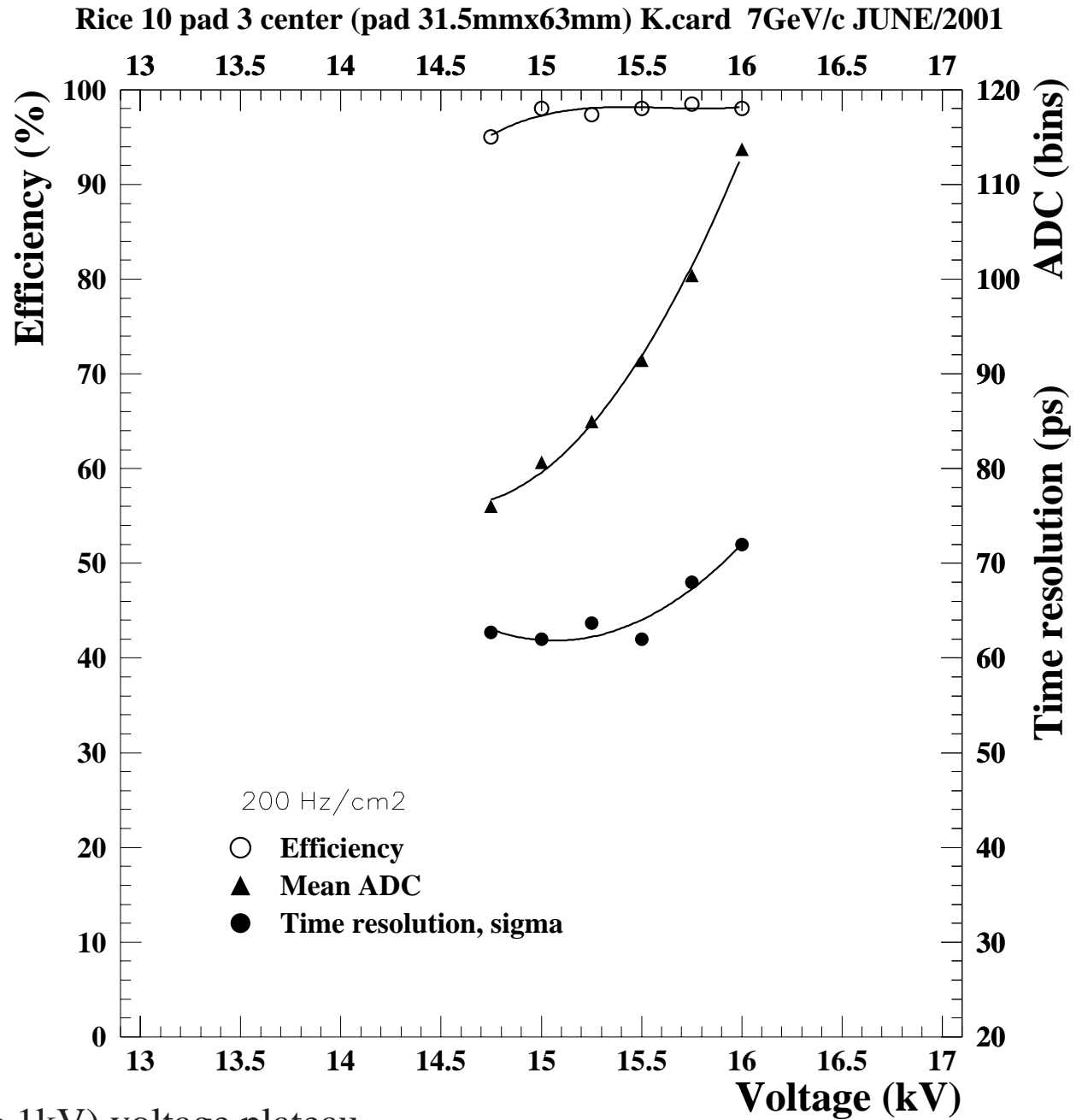
- new technology - adopted also by ALICE, operated in HARP experiment at CERN PS...
- versions for use in STAR developed by Rice group working closely w/ ALICE (1998-2001)...
- orders of magnitude cheaper per detector channel than mesh PMTs...
- relatively easy to fabricate...



applied potential  $\pm 7-8\text{kV}$

gas typically 90% Freon R134A, 5% isobutane, 5% SF<sub>6</sub>

MRPC results from  
CERN test beams  
(1998-2001)



~98% efficient over a wide (>1kV) voltage plateau...

~60-70 ps pure stop resolution are typical...

→ the MRPC technology (here as the Rice v.10 design) easily meets the requirements for STAR

**STAR TOFr** the first full-sized implementation of an MRPC-based TOF tray for STAR...

*Feb. 2002*

first power up, noise rates  $\sim 50\text{Hz}$ , current draw  $\sim 1\text{nA/module}$  (6ch) at full voltage...

*Spring 2002*

full tray testing in AGS radiation area, stable operation for 70 days...

*Fall 2002*

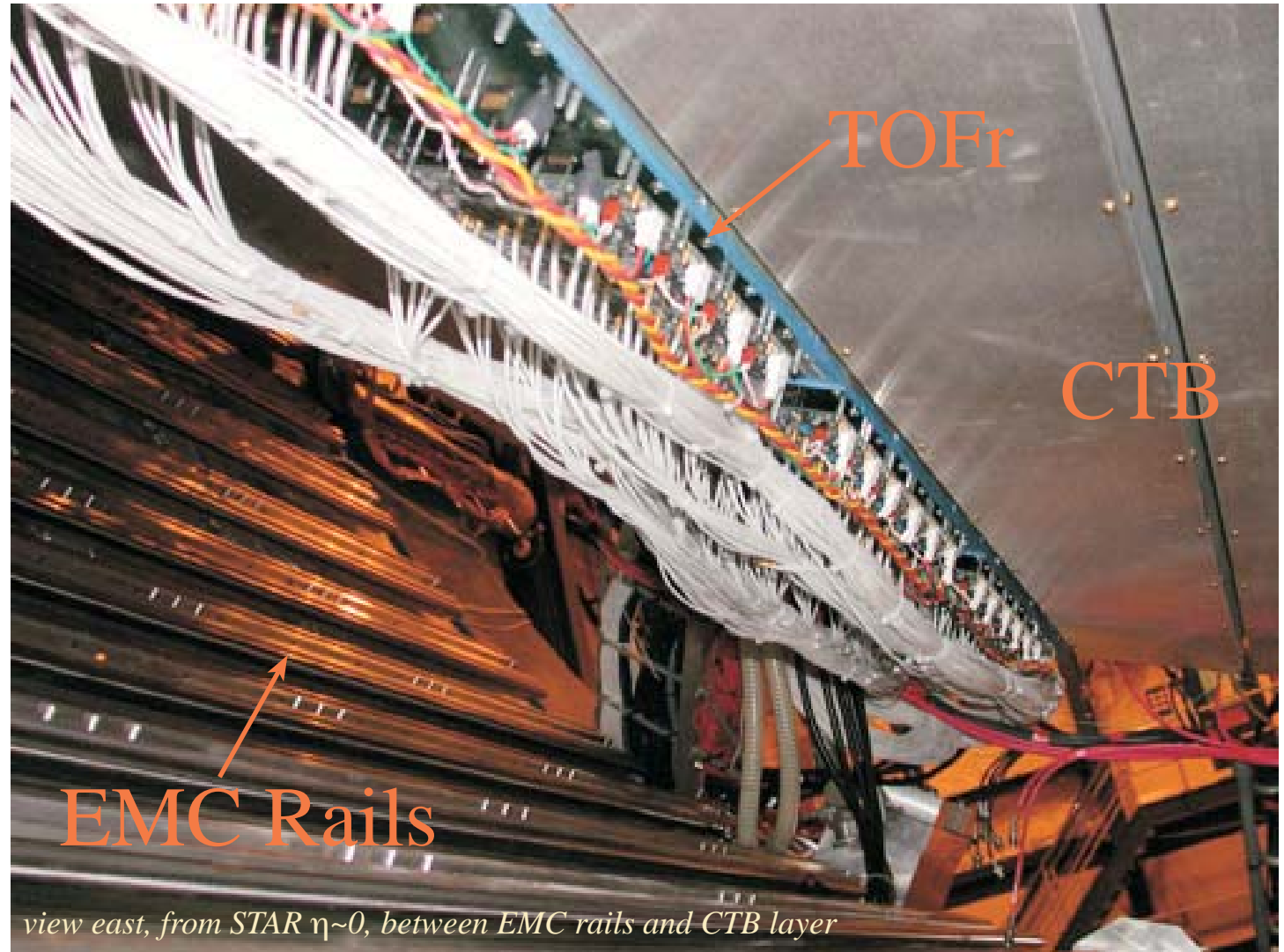
Installed in STAR  
Ready for Run-III

note TOFr exceeds it's  
integration limits!

*(TOFr height  $\gg$  CTB's!)*

→ must make significant  
modifications to tray  
design and size/shape of  
the electronics layer!

→ one of the important  
overall goals of the  
proposed FY03 R&D



by the end of RHIC Run III, **optimal HV&Threshold settings** for a few gas mixtures,  
timing **performance**, occupancy and **the proof of principle**  
from the extended operation in the most realistic environment possible....

The design of the MRPC detectors for STAR has been final for ~1 year...

Basic aspects of FEE (amplification and discrimination) understood  
basic design of TOFr FEE appears (so far) to work fine...

However, a common element of  
the STAR TOFp system,  
the 1998-2001 test beams and development of the MRPC detectors for STAR,  
the TOFr tests at the AGS,  
the TOFr testing in STAR during RHIC Run-III,  
is that **the electronics used are not applicable** for use in a large-area TOF system in STAR...

All of the major technical challenges remaining thus relate solely to **THE ELECTRONICS....**

FEE must be compact, *i.e.* approximately the same area as a MRPC cell (~3x6cm)

Digitization must be done locally, *i.e.* must also be compact

Start and stop detectors digitized w/ the same electronics

Versus a common distributed clock

MRPC signals are *fast*

MRPC signals are *small*, ~25 fC per hit!

amplification necessary (trade-offs between bandwidth and jitter/design complexity)

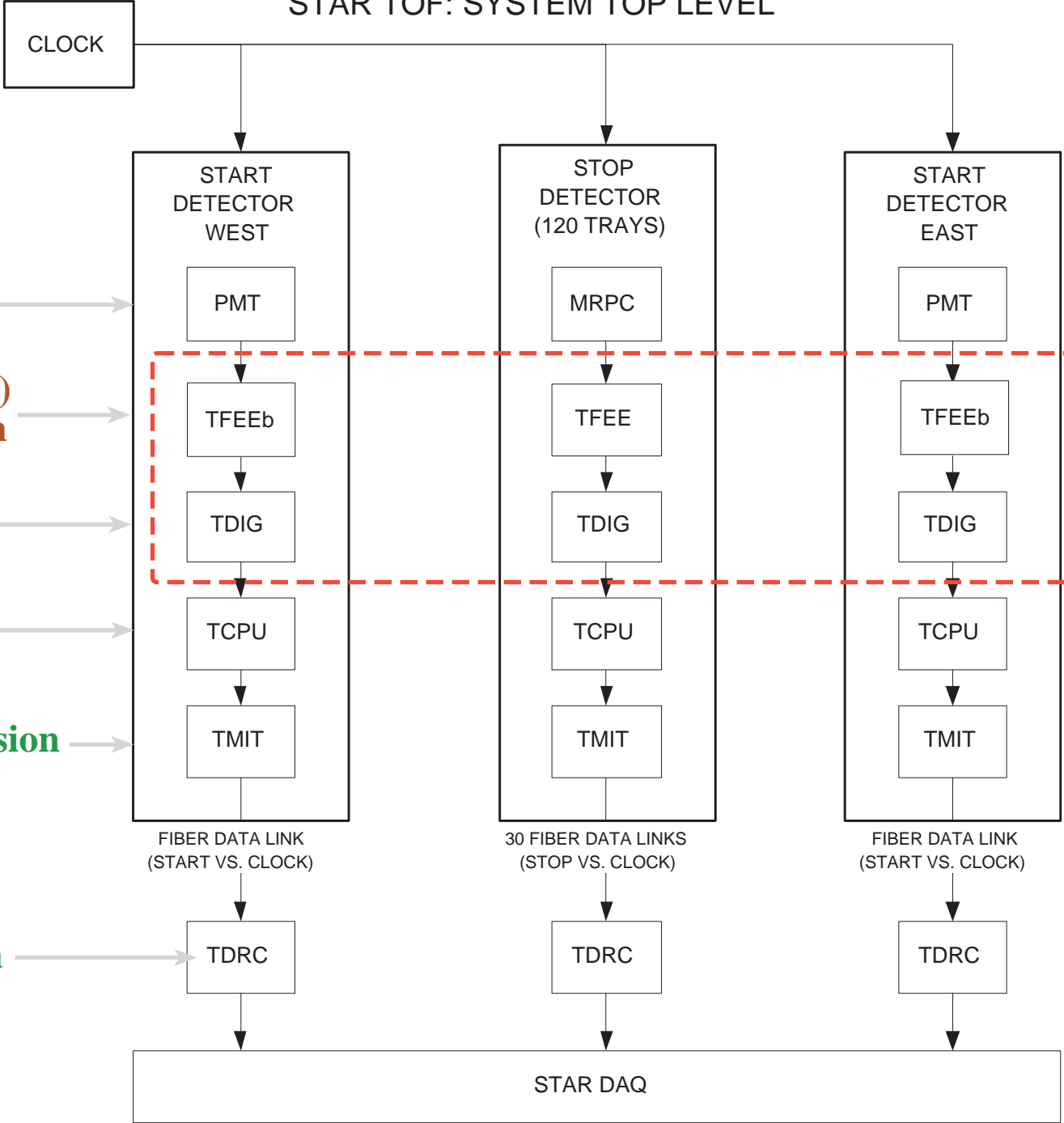
high sensitivity to noise (especially RF, requires careful integration of electronics and gas volume)

FEE via discrete components has worked well so far,  
but improvements possible (in performance and/or cost and/or design complexity).

No commercial options exist for the digitization.



STAR TOF: SYSTEM TOP LEVEL



.....on-detector.....

in DAQ room

**detectors**

**(amplification)  
discrimination**

**digitization**

**buffering  
formatting**

**data transmission**

**data reception**

...the major technical challenges...

(not shown: TRG word information to TDIG, TOF mult info to TRG DSMs)

## Phase-I SBIR 70460S02-I

“A Time of Flight Data Acquisition System for Ultra-Fast Particle Detectors”

*L. Bridges (P.I.), T. Nussbaum, W.J. Llope, B. Bonner*

- 100k\$ for 9 months from August 2002 - March 2003.
- Goal: **First generation TDIG prototype** based on HPTDC chip: “**JALEPENO**”  
First testing/**communication with HPTDC chip**

**R&D funding is needed for FY03 (128k\$) and FY04 (134k\$) to attack major unknown areas in the design of the TFEE and TDIG components of the STAR TOF electronics chain...**

### FY03 Scope & Deliverables:

#### 1. **Final specification of Amplifier and Comparator for TFEE...**

- **TOFr FEE: Maxim 3760 amplifier** (also enthusiastically adopted by ALICE) - 600 MHz  
Need to investigate newer models... (cheaper at same performance?)  
and Higher bandwidth models (1-1.2 GHz).. . (faster leading edges at comparator?)  
and Monolithic Microwave ICs (MMICs)... (better impedance matching?)
- **TOFp and TOFr FEE: AD96687 comparator** - ECL outputs, HPTDC wants PECL inputs  
Need to investigate newer models... (simpler TFEE design? less jitter?)

#### 2. **First generation prototype of TFEE based on final amplifier & comparator...**

first important step towards better suppression of RF noise...

to be installed on TOFr' in advance of RHIC Run IV for testing in STAR environment

### FY04 Scope & Deliverables:

3. **Second generation prototype of TDIG, based on experience gained during Jalapeno SBIR...**
4. **First successful configuration of the HPTDC-equipped TDIG prototype, strict performance testing...**
5. **First attempts at operation of the full chain of MRPC → TFEE prototype → TDIG prototype...**

## Manpower committed to this R&D:

T. Nussbaum	Electrical Engineer	100% FTE	(supported by R&D funds)
L. Bridges	Electrical Engineer	50% FTE	(supported by Phase-I SBIR funds)
W.J. Llope	Physicist	50% FTE	(from Rice U. base)
G. Eppley	Physicist	50% FTE	(from Rice U. base)
F. Geurts	Postdoc	20% FTE	(from Rice U. base)
J. Schambach	Physicist	75% FTE	(from U. Texas base)
J. Hoffmann	Physicist	25% FTE	(from U. Texas base)

## Anticipated Costs:

FY03	FY04		
64 k\$	68 k\$	Salaries (includes fringe)	only for personnel supported by R&D funds (Nussbaum)
38 k\$	39 k\$	Overhead costs	only for personnel supported by R&D funds (Nussbaum)
12 k\$	12 k\$	Travel	to beam-test facilities, and to visit ALICE at CERN
14 k\$	15 k\$	Purchases	for prototypes and test beam supplies
<b>128 k\$</b>	<b>134 k\$</b>	<b>Totals</b>	

## Milestones:

- 3/15/03** Completion of amplifier/comparator testing → finalize TFEE components...
- 10/1/03** Completion of first prototype TFEE → install on TOFr in advance of RHIC Run IV...
- 12/1/03** Completion of second prototype of TDIG...
- 4/1/04** Successful configuration of HPTDC chip, performance comparisons to CAMAC *etc...*
- 10/1/04** Successful operation of proto-chain: MRPC → TFEE prototype → TDIG prototype

Details on proposed R&D towards STAR-TOF TFEE and TDIG electronics  
t. nussbaum, w.j. llope  
12/12/2002

The TOFp system has 41 channels of local FEE in-tray that are based on the Analog Devices AD96687 dual comparator. The same TOFp FEE boards are used without modification in the two pVPD (start) detectors. During RHIC Run II, the performance of these FEE on both the start and stop sides met the requirements as the overall system timing resolution was sub-100ps and charged hadron PID reached to the expected momentum limits. The TOFr system has ~180 channels of local FEE on-tray that are based on the same comparator, but also include the Maxim 3760 pre-amplifier to handle the very small (~25 fC) MRPC signals. For both systems, the jitter of these FEE on the bench was ~20ps (near the limit we can measure it with an 8 GSa/s HP Infinium oscilloscope). We thus expect the same good performance from this comparator when TOFr is operating during the upcoming RHIC Run III. The FEE for the TOFr are mounted to the tray in a complicated manner involving ~300 screw posts and a separate layer of feedthrough plates which close the gas volume.

Low voltage (+/-5V for TOFp, +/-6.5V for TOFr) from platform-mounted power supplies is distributed to these on-detector FEE via ~120ft of 5-conductor 10AWG VNTC cable. As the TOFp and TOFr FEE draw 10-20A when fully powered, the voltage drop along these cables is significant and overvoltage is required on the platform. For a full system of 120 trays, the heat generated over 120\*4 10AWG copper cables carrying ~10-20A is not negligible. Simplifications of the LV requirements in the first prototype of the TFEE and TDIG combination would thus allow a simpler, lower power, LV distribution system and less heat in the Wide Angle Hall. Comparators other than TOFp/r's AD96687 may be better matched to the MRPC technology leading to performance improvements, and may also allow important reductions of the board complexity and cost. Amplifiers other than TOFr's Maxim 3760 may also lead to important performance enhancements related to amplifier bandwidth and potentially better impedance-matching to the MRPC detectors. Given the extremely small size of the MRPC signals, the proper choice of amplifier for the TOF FEE is critical. The best-possible suppression of noise, especially RFI, is likewise critical. This calls for the replacement of TOFr's two layers of feedthrough plates plus FEE with one layer of TFEE boards that make the box gas-tight and also more RFI-tight.

The following provides additional technical details on the R&D to be performed towards the first prototype of a realistic TFEE board for the full system.

Comparators:

The Analog Devices AD96685,7 comparator we use now in ToFp,r has ECL output (-.85 to -1.85 volts). This is not easily compatible with LVDS inputs on the CERN HPTDC. The obvious solution, addition of a logic level translator stage is undesirable due to added circuit complexity, power and possible increase in jitter. It has been demonstrated that by shifting the ground and the two power supply pins up by ~2.5 volts that it could be made to work fine without logic level translators. The disadvantage for our large scale system is that power distribution (+7.2, +2.5, -3.2) probably becomes too complex & inefficient.

Last spring Maxim announced the Max9601 device with Positive ECL outputs which when attenuated by double termination (source & load) will be acceptable to the LVDS inputs on HPTDC. It has a much lower propagation delay (.5ns vs 2.5ns) and dispersion (30ps vs 50 ps) than AD96685 which implies a much higher bandwidth. There is also an adjustable Hysteresis function which could be useful in controlling oscillations for the implementation of the Time Over Threshold circuitry needed for the offline slewing corrections. Standard power supply voltages of this device are +5.2 & -5.0. It has been confirmed with Maxim Technical Support that no performance degradation should occur in using supplies of +3.0 & -7.2 volts. This would not introduce power distribution inefficiency of having to regulate down to 3 volts for the preamp and TDIG power. Cost in 1k volumes is \$4.50, or \$2.25 per channel.

A third idea was to use Max3264 "Limiting Post Amplifier" which is essentially a comparator used to discriminate Fiber Optic receiver signals before deserialization. The big advantage of this device is that it only needs +3 volts and the CML outputs can be easily made compatible with HPTDC by resistive dividers and biasing. Feeding in the discrimination threshold is slightly more complex in this case because it needs to be done differentially and there is an internal input termination resistor. A practical circuit to

do this was devised and tested, where it demonstrated an excellent timing performance with a preamp signal driven by a fast pulser. The disadvantage of this device is its high cost (\$8.60 per channel). This is probably more than would be saved on power supply cost alone, but the additional savings in the wiring, connector costs, and circuit complexity make it worth considering further.

Preamps:

In addition to proving acceptability of newer, low power 3 volt replacements to MAX3760, significantly higher bandwidth devices of that type or the MMIC family also used in a differential (dual preamps per MRPC pad) configuration could reduce the magnitude of the slewing effect. The thinking is that susceptibility to RFI and self oscillation should be much lower with the differential (dual preamp per pad) input and better grounding of the FEE as an integral part of the gas box. Assuming the MRPC noise distributions allow it, the discriminator threshold could then be set much lower and result in an improved detector efficiency. The channel-to-channel variations also become less significant.

The advantage for MMIC devices is that input impedance is inherently matched to the 100 ohm twisted pair cables that bring the MRPC signals to the FEE. Actual testing with MRPC signals seems to be the only way to evaluate the advantages of this and other effects, e.g. noise and jitter.

An implementation of the differential configuration with MMICs would require 4 devices per MRPC channel to get enough gain. These are physically very small (~.08"x.08") and low cost (~\$6.00 per channel). They are also low-power 3 volt devices. The impact on the complexity and reliability of the circuit design and assembly is not expected to be severe. A potential disadvantage is that the specified channel-to-channel gain variation is much higher than with the Max3760-type devices (~3:1 vs. ~1.6:1).

Differential implementation with lower power and higher bandwidth Max3760 type devices may also be practical if the gain variation versus bandwidth trade-off is not favorable for MMIC devices. The new low power devices (.12"x.2") are much smaller than the current MAX3760 (.244" x .197") where two are being required per channel at ~\$10 each.