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Simple front-end electronics for multigap resistive plate chambers

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ABSTRACT

A simple circuit for the presentation of the signals from Multi-gap Resistive Plate Chambers (MRPCs) to standard existing digitization electronics is described. The circuit is based on "off-the-shelf" discrete components. An optimization of the values of specific components is required to match the aspects of the MRPCs for the given application. This simple circuit is an attractive option for the initial signal processing for MRPC prototyping and bench- or beam-testing efforts, as well as for final implementations of small-area Time-of-Flight systems with existing data acquisition systems.

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1. Introduction

The Time-of-Flight (TOF) systems for the ALICE [1] and STAR [2] experiments are large-area systems based on Multigap Resistive Plate Chambers (MRPCs). The large channel counts of these systems demand that the front-end electronics (FEE) and digitization are done "on-detector." The electronics for these systems are based on the NINO chip [3] for the amplification and the HPTDC chip [4] for the digitization. For smaller TOF systems, as well as MRPC prototype testing with cosmic rays or at test-beams, simpler FEE read-out by an existing data acquisition system can be a productive approach. Such electronics are inexpensive, simple to develop, low power, and quick and easy to construct out-of-house. An example of such electronics, which properly amplify the very small signals from MRPCs and drive 50 Ω signal cables to the digitizers, is described here. This circuit is based on readily available "off-the-shelf" discrete components.

Boards of this type are presently in use as the FEE for the new PHENIX "TOF-west" system [5], as well as the prototype Muon Telescope Detector (MTD) [6] in the STAR experiment, both at the Relativistic Heavy-Ion Collider (RHIC) at Brookhaven National Laboratory (BNL). An earlier version of this circuit was used for the STAR TOF prototype "TOFr" [7] in RHIC Run 3 and in a test-beam, as well as presently in the cosmic test stands used to qualify newly constructed STAR TOF MRPCs at the detector fabrication sites in China [8]. Similar electronics were used during the prototyping of the ALICE [9] and TOF detectors.

This paper is organized as follows. Section 2 describes the circuit and its optimization for the present applications using bench data. Section 3 presents the summary and conclusions.

2. Circuit description

MRPCs are highly capacitive detectors (10–20 pF) that produce very small signals (~50 fC). In order to produce output signals large enough for digitization after long cables in typical data acquisition systems, significant pre-amplification and subsequent amplification of the signals is needed. The overall current gain of these electronics into a 50 Ω load is a factor of ~500. This large amount of amplification assumes a careful and complete shielding of external radio-frequency noise. To achieve this shielding, these electronics exist as two layers of electronics boards. A "feed-through" (FT) board and a FEE board. The FT board bolts to the exterior of the aluminum gas volume that encloses the MRPCs in a way that insures a low-impedance connection between the enclosure ground and the electronics ground. The FT boards thus serve to close the MRPC gas volume as well as complete a Faraday cage around the MRPCs. The FT boards pass the detector signals to the FEE boards.

An air gap between the FT and FEE boards insures that the power dissipated in the FEE board does not radiatively heat the MRPCs inside the gas volume, which would increase the MRPC noise rates and high voltage currents. The capacitance of MRPCs is an order of magnitude larger than that for the typical industrial

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applications of the pre-amplifiers used in these electronics. This requires an optimization of the "matching" of these electronics to the MRPCs. Also, the feed-back circuitry around the amplifier controls the overall gain and bandwidth (signal rise-time) and requires an optimization tailored to the specific application. These optimizations are accomplished via the selection of the values of specific resistors in the circuit. In practice, prototype versions of these electronics were constructed and then tested with cosmics or test-beams using the specific MRPCs for a given application. Different channels of these prototype boards were configured to use different values for these resistors. This allowed the collection of the test data needed to optimize these settings. Once the preferred settings were determined, the final board production was begun.

The basic circuit of the FEE board is shown in Fig. 1. Each FT and FEE board handles a total of eight MRPC read-out channels. The MRPC signals are brought from the MRPC pads to the underside (inside the gas volume) of the FT boards via twisted-pair ribbon cables. "Samtec" connectors [10] were used to bring the MRPC signals to the inputs of the FEE boards. These "low-profile" connectors were required due to the very tight integration volume for the PHENIX TOF-west implementation. The vertical spacing between the top of the FT board and the underside of the FEE board is $\frac{3}{16}$ inch and is controlled by threaded hex stand-offs on the 4–40 "PEM stud" threaded posts mounted on the detector gas volume. These same low-profile connectors were also used for the STAR MTD prototype.

The MRPC signals enter the FEE boards on the left side of Fig. 1. The input labelled "IN+" is connected to the side of the MRPC to which positive high voltage is applied, while the input labelled "IN−" is connected to other side of the MRPC. This results in negative-going signals derived from the anode read-out electrode of the MRPC at the inputs of the FEE boards. The FEE output signals, which are also negative, are available at the right side of this figure. Each FEE board has six planes — two ground planes, two voltage planes, and two routing planes, although only one routing plane was actually used.

The first components, the resistors R16, R20, and R21, deal with the extremely reactive behavior of the MRPCs and their twisted pair signal leads as a function of the (Fourier) frequency of the input pulses. The capacitance of the signal cable leads is 15 pF/ft or 10 pF for 8 inch. These need to be considered as distributed element twisted-pair transmission lines. Over the bandwidth of interest (500 MHz), the impedance of the combined circuit consisting of the 8 inch transmission line and the MRPCs goes from being that of a $(10 + 7) = 17$ pF capacitor at low frequencies, through a resonance at ~160 MHz where the impedance is zero, to an inductive reactance (negative "capacitance") at higher frequencies. By design, the pre-amplifier used here prefers input capacitances below 1 pF, which is at least an order of magnitude below that for these MRPC inputs. While these resistors do attenuate the input signals, the desired effect is to make the MRPC and its twisted pair signal cables appear less reactive at the input to the pre-amplifier to reduce its instability and ringing. The residual ringing still due to the internal feedback design of the pre-amplifier was judged acceptable in these applications as the pulse area (via Analog to Digital Converters in the digitization system), not its "time over threshold," is used as the independent variable for the offline pulse slewing [11] corrections.

The resistors R16, R20, and R21 also properly terminate the twisted-pair signal cables coming from the MRPCs. As MRPCs are capacitive, the smallest possible impedance of the signal cabling and the FEE is desirable as it results in the fastest rise-times of the output pulses. Thus, two twisted-pairs per MRPC read-out channel were used to bring the signals to the FT boards. Additional details on the optimization of these resistor values are provided below.

The next component, labelled D3, is the Schottky diode "hsms2822" from Agilent, which provides the input voltage protection to the rest of the circuit. Input pulse heights above ~400 mV are cropped at this height. This effectively never occurs, as this value is two orders of magnitude higher than the detector pulse heights.

The detector signal then enters a Maxim 3664 transimpedance amplifier (the "pre-amplifier") which converts the current pulse from the detector to a differential voltage proportional to the input pulse current. The advantage of the Maxim 3664 transimpedance pre-amplifier is its much higher and more consistent (±10%) gain compared to that for Monolithic Microwave Integrated Circuit (MMIC) pre-amplifiers, which were also considered for the present circuit. The Maxim 3664 reduces the number of stages and the channel-to-channel gain variations via the feedback design.

A comparison of the linearity of the FEE boards with two different transimpedance pre-amplifier chips is shown in Fig. 2. The horizontal axis is the pulse height from a pulser. The pulser output is heavily attenuated (~40 dB) before it is input to the FEE boards. The two point styles indicate the pulse height output from the FEE board when using the Maxim 3760 or the Maxim 3664 pre-amplifier. The signal termination included in the board with the MAX3760 chip prevents a direct comparison of the intrinsic device gains, which, according to their specifications, are equal. The two curves have thus been normalized at 2 V. However, it can be seen that the linearity of the MAX3664 is noticeably better than that of the MAX3760 over the same range of input pulse heights.

The differential voltage from the Maxim 3664 pre-amplifier is then sent to an Analog Devices AD8001ar operational amplifier.

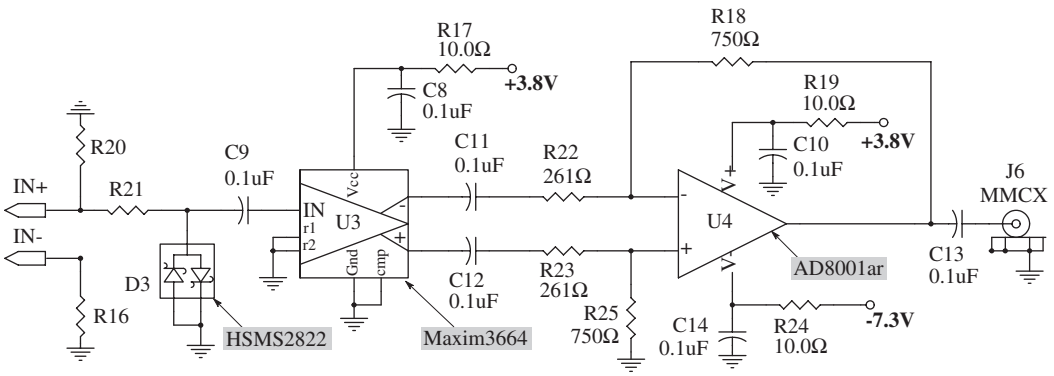

Fig. 1. The components of the present circuit.

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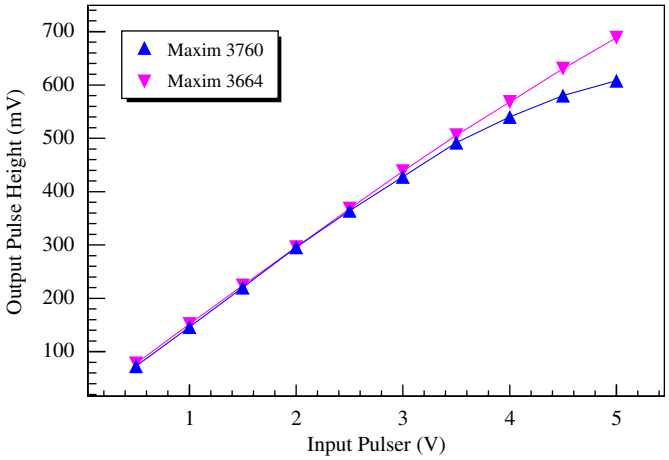

Fig. 2. The output versus (attenuated) input pulse height for the pre-amplifiers used in the prototype and final electronics.

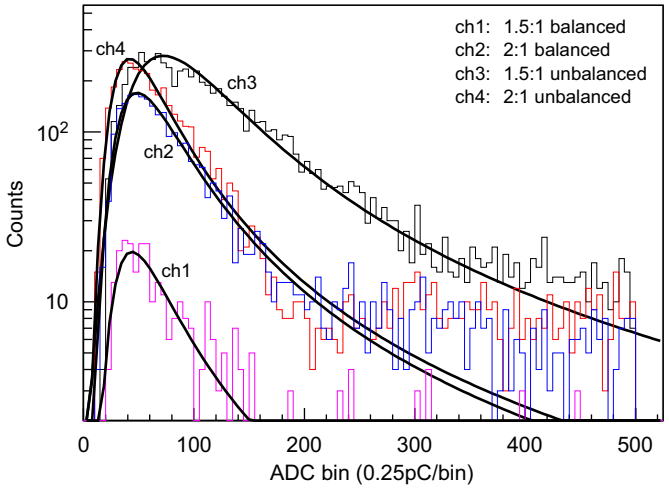

Fig. 3. The pulse-area distributions for a number of values of the impedance-matching resistors R16, R20, and R21 obtained with a PHENIX TOF-west prototype MRPC.

This drives the output signals to be sent over long coaxial cables to the digitizers. The resistors R18 and R22 and R23 are part of the "feedback" network for this amplifier. The ratio of the values of R18 to R22 and R23 changes the overall output gain, while the absolute value of the resistor R18 changes the bandwidth (rise-time) of the output. The shortest achievable output rise-times are clearly of primary interest for the ultimate timing of the detectors, especially in the presence of long cables before the digitizers.

The pre-amplifier requires only a positive input voltage, while the amplifier requires both positive and negative voltages. The rise time of the pulses out of the amplifier are the fastest when the absolute difference between the positive and negative voltages is on the order of 10 V. The best results were obtained by setting the pre-amplifier voltage to +3.8 V, and the amplifier voltages to +3.8 V and −7.3 V. These bipolar asymmetrical power supplies also minimized the power dissipation in the voltage regulators (not shown in Fig. 1). The currents drawn per board are approximately 240 and 40 mA on the positive and negative inputs, respectively. In accordance with typical safety requirements at BNL, all power inputs are independently protected with 0.75 and 0.3 A fuses, respectively.

The resistor (10 Ω) and capacitor (0.1 μF) pairs R17 and C8, R19 and C10, and R24 and C14, provide the power supply filtering for the suppression of cross-talk across read-out channels. The timing cross-talk for these boards was measured with a pulser and an 8 GSa/s Hewlett-Packard (now Agilent) Infinium oscilloscope and was seen to be less than 10 ps (*i.e.,* lower than experimentally measurable).

Finally, the capacitor C13 "AC-couples" the FEE to the digitization electronics. This eliminates the possible degradations to the performance from ground loops in the final implementation of these electronics. The output is the "MMCX" connector, J6. This connector was chosen because of its very small size (and PHENIX's very tight integration volume). An RG-316 type coaxial cable connects to this location and brings the outputs to the digitization electronics for the pulse area and timing measurements.

Once the basic circuit was developed, a few prototype boards were built and delivered. In different channels of these prototype boards, different values of the initial "impedance matching resistors" R16, R20, and R21 were used. Data were then collected with the PHENIX TOF-west MRPCs and the resulting gain of the FEE compared across these test channels. The result is shown in Fig. 3. In the "balanced" configurations, the value of the resistor R16 was set via $1/R_{16} = 1/R_{20} + 1/R_{21}$, while in the "unbalanced" configurations, the resistor $R16$ is removed and this side of the MRPC output (IN−) goes directly to ground. The labels "1.5:1" and "2:1" denote the attenuation of the MRPC signal current from the IN+ side of the MRPC, which is given by the ratio $[R_{20} + R_{21}]/R_{20}$. On the basis of Fig. 3, the "1.5:1 unbalanced" configuration was chosen, as this resulted in the largest mean-value of the digitized pulse areas across the various test channels. The resistor values thus chosen for the final production were $R_{16} = 0$, $R_{20} = 174\,\Omega$, and $R_{21} = 75\,\Omega$. The mean pulse areas seen in this figure for the chosen resistor configuration is approximately 100 ADC channels (25 pC). For the factor of 500 current gain of these electronics, this implies the input pulse areas are of order 50 fC.

Using an attenuated pulser with a ∼0.3 ns rise-time, the 10–90% rise-time of the output signals is 1.35 ns. The "peaking time" is 2 ns.

3. Conclusions

A simple circuit based on readily available discrete components was developed for MRPC detectors. These boards are simple enough that they can easily and reliably assembled "out-of-house". These electronics are presently in use in the PHENIX TOF-west system and the STAR Muon Telescope Detector prototype. The ultimate timing performance of these systems following the offline corrections, which will be described elsewhere, met expectations.

Acknowledgments

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